SHARING

SELF-ORGANIZED HETEROGENEOUS ADVANCED RADIO NETWORKS GENERATION

Deliverable D7.4

Final proof of concept validations, results and analysis

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Editor(s)	Yolanda Fernández (TTI)
Author(s)	Yolanda Fernández (TTI), Adrián Sánchez (TTI), Vincent Berg (CEA), Marc Laugeois (CEA), Sylvie Mayrargue (CEA), Engin Zeydan (AVEA), A. Serdar Tan (AVEA), Amor Nafkha (SUP), Dominique Nussbaum (EUR)
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Abstract:

This document describes the final validation of the proof of concepts developed by SHARING project, thereby giving an illustration of the main project achievements. Five different proof-of-concepts were developed related to the following topics:

- Relaying and Device-to-Device communications
- Interference aware receiver of downlink MU-MIMO coordinated multi-point
- Carrier aggregation
- Wi-Fi offloading
- FPGA reconfigurability for low-power APT-VDF filter implementation

This deliverable provides the results and analysis of the concomitant trials.

Keywords: eMBMS multicast-broadcast services, Device-to-Device, Cooperative Multipoint, Multi-user MIMO, Interference Aware receiver, Carrier Aggregation, Wi-Fi Offloading.

Document Revision History

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0.1	18/11/2015	TTI	Creation of the Table of Contents (ToC)
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0.10	29/01/2016	TTI	First stable version
1.0	10/02/2016	TTI	Final version

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EXECUTIVE SUMMARY

In SHARING Deliverable D7.3 "Integration of selected implementations into platforms & interfaces finalization" [1], the proof-of-concepts were described together with the required interfaces. Moreover, initial test results of the implementations were presented.

Now this document shows in detail the final results and analysis of the trials related to the selected topics in D7.3 [1]:

- Relaying and Device-to-Device communications (D2D) (WP5)
- Interference aware receiver of downlink MU-MIMO coordinated multi-point (CoMP) (WP3)
- Carrier aggregation (WP3)
- Wi-Fi offloading (WP4)
- FPGA reconfigurability for low-power APT-VDF filter implementation

This document describes the final validation of the developed proof of concepts, thereby giving an illustration of the main project achievements. Trial set-ups are described below:

Relaying and Device-to-Device communications

Two implementation scenarios covering eMBMS relaying and D2D transmission are proposed. The first one corresponds to the case of a macro-cell eMBMS transmission which is relayed on a secondary component carrier to the region around the relay. The second scenario corresponds to the case where UEs with storage capabilities are used as relays. In this scenario UE-relays broadcast their content to their local vicinity under the command of the eNB which represents at least one Public Land Mobile Network (PLMN) which is aware of the content in the UE-relays. Hardware and software implementation details and interfaces are defined based on the OpenAirInterface (OAI) platform (www.openairinterface.org). The implementation in a real environment (around the EURECOM premises) is considered in this report.

Interference aware receiver of DL MU-MIMO CoMP

Two different algorithms were considered for interference mitigation: SL-MMSE and IAML. The scenario consists of two UEs benefiting from the cooperation of two eNBs in Joint Processing/Joint Transmission (JP/JT) mode; each eNB being under MU-MIMO Transmission Mode 5 (TM5) of the 3GPP LTE. The complexity of the implementation was evaluated for a 4x4 transmission channel (4 antennas at the UE, which is a reasonable assumption for future terminals, and 4 antennas at each base station). Furthermore, the methodology is generic and valid for any NxM configuration.

We conclude that the "QR + linear system solving" solution is more complex (over 30%) than direct matrix inversion. However the computational time is reduced by 60%. Therefore depending on the overall system complexity and computational time requirements, the solution should be chosen.

Carrier aggregation

The scope of this implementation refers to a small cell scenario where carrier aggregation (CA) is implemented. Two different hardware prototypes were jointly developed: a reconfigurable and flexible bandwidth RF front-end and a multi-band frequency agile antenna. Both demonstrators support intra-band CA at LTE band 7 and inter-band CA at LTE band 20 and LTE band 7.

The reconfigurable and flexible bandwidth RF front-end is capable to work at different operating points which are optimized according to the number of component carriers (CCs) and CA configuration to improve energy efficiency (compared to single operating point operation). An energy efficiency evaluation was carried out defining 17 dBm as the average power per CC associated to the most restrictive CA configuration for this demonstrator (namely3CCs in intra-band contiguous CA). Energy efficiency improvement is calculated comparing the results at 28V operating point and the results at optimized operating points. For 2CCs in intra-band contiguous CA, energy efficiency enhancement is around 25% and between 35-39% in intra-band non-contiguous CA. Achieving up to 50% for only 1CC.

The multi-band frequency agile antenna was integrated jointly with the RF front-end presenting a very high performance in terms of gain despite its miniaturization. Both prototypes were validated performing a radio link among the small cell base station and an auxiliary antenna which emulates the user equipment antenna. Different CA configurations were tested and it checked that both prototypes are proper to support CA.

Wi-Fi offloading

The proof-of-concept is an integrated Wi-Fi offloading platform in mobile operator networks which uses a multiple attribute decision making (MADM) algorithm for efficient Wi-Fi offloading in heterogeneous wireless networks. The platform collects several terminals and network level attributes via infrastructure and client APIs and decides on the best network access technology to connect for requested users. The centralized connectivity management server is called SHARING server and runs a MADM algorithm called TOPSIS. A simplified demonstration was performed demonstrating system level optimization. From the experimental evaluations based on the sensitivity of the weights of the MADM algorithm, operators acquire knowledge to adapt Wi-Fi offloading platforms into their network infrastructures.

FPGA reconfigurability for low-power APT-VDF filter implementation

FPGA dynamic partial reconfiguration (DPR) is an advanced design technique. It can be used as an effective power reduction technique in reconfigurable computing systems. To improve the hardware implementation of new technologies and advanced techniques, the DPR can be used to perform run-time hardware reconfiguration. In SHARING project, the DPR design technique can be used to implement reconfigurable filter-bank, reconfigurable interference aware receiver, etc. In this deliverable, a reconfigurable, low-complexity all-pass transform variable digital filter (APT-VDF) was designed on FPGA platform. The main objective is to implement this filter using FPGA dynamic partial reconfiguration technique which allows very low power consumption and a reduced reconfiguration time. The implemented filter is capable of extracting channels of uniform bandwidths. Experimental measurements of power consumption for core logic of Virtex5 FPGA, during total and partial FPGA reconfiguration, are presented.

1 INTRODUCTION

This document describes the final validation of the developed proof of concepts, thereby giving an illustration of the main project achievements.

Previously in SHARING Deliverable D7.3 "Integration of selected implementations into platforms & interfaces finalization" [1], the proof-of-concepts were described together with the required interfaces. Moreover, initial test results of the implementations were presented.

Now this document detail the final results and analysis of the trials related to the following topics:

- Relaying and Device-to-Device communications
- Interference aware receiver of DL MU-MIMO CoMP
- Carrier aggregation
- Wi-Fi offloading
- FPGA reconfigurability for low-power APT-VDF filter implementation

2 VALIDATION OF SELECTED IMPLEMENTATIONS

2.1 Relaying and D2D (EUR)

2.1.1 Description

We will consider two demonstration scenarios as described in Figure 1 and Figure 2, with priority given to the eMBMS relaying. These scenarios are described in more detail in [1].

The first use case corresponds to the case of a macro-cell eMBMS transmission which is relayed on a secondary component carrier to the region around the relay. The relays derive time and frequency synchronization from the macro-cell eNBs and have transmit-only functionality. The relay is a decode-and-forward relay made up of a standard eMBMS-aware UE and the eMBMS TX-path of an eNB. These ensure coverage of the primary eMBMS carrier in difficulty to reach areas such as large underground zones or heavily shadowed zones, which would limit the global eMBMS throughput if covered by the macro-cell eNB only. The primary target is to serve the MBSFN-area with a very high-spectral efficiency from the macro-cell eNBs which are received by the great majority of locations and add the TX-only relay to cover the difficult-to-reach zones.

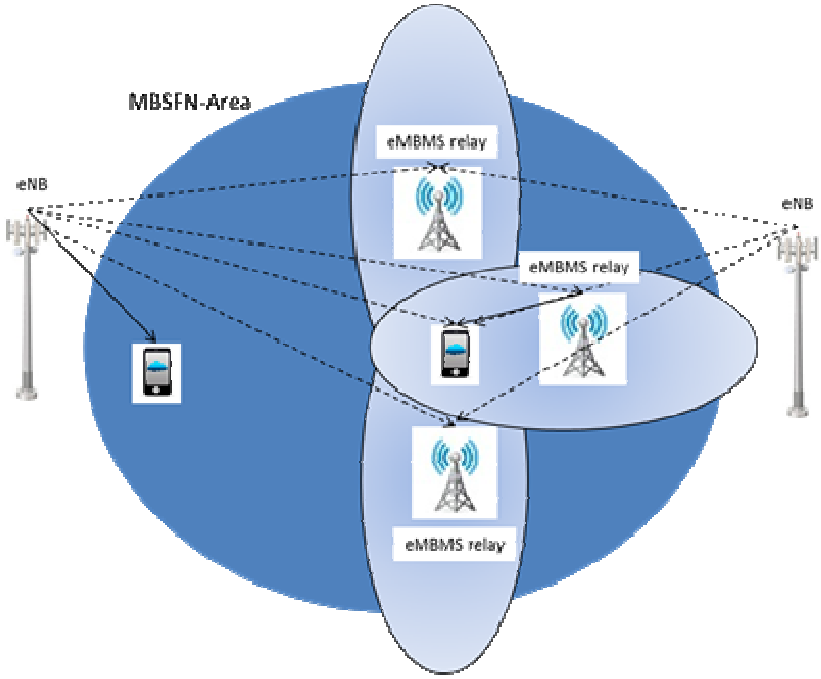


Figure 1 Use case 1: eMBMS Relay (dual-carrier)

The second use case in Figure 2is more representative of a D2D scenario but can be demonstrated on a similar platform than the first use-case. Here we assume UEs with storage which can be used to offload their content to their local vicinity under the command of the eNB which represents at least one Public Land Mobile Network (PLMN) which is aware of the content in the UE relay. The key innovation here is to exploit the uplink carrier for D2D content offload without significantly disturbing the eNB's receiver link budget. All UEs must be able to listen to both the downlink and uplink carrier simultaneously, in FDD and TDD.

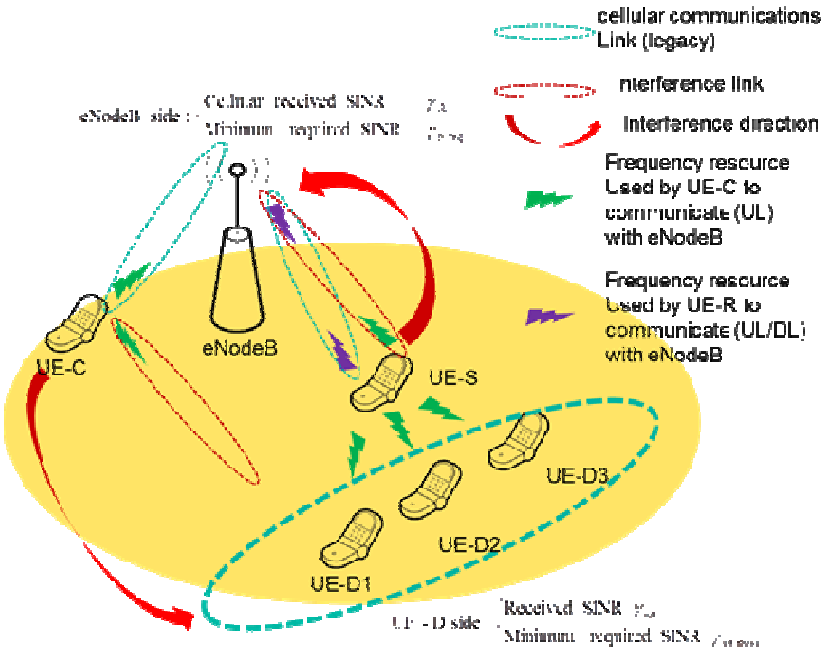


Figure 2 Use case 2: Content delivery (via proximity-based D2D broadcast)

2.1.2 Validation results

This section depicts the experiments that have been conducted in the frequency bands where EURECOM is allowed to transmit (authorization by the ARCEP, the French regulator). Those experiments have been conducted near the EURECOM Building, in Sophia Antipolis, France. The objectives of the tests are:

- To test the basic functionalities of the platform (TX, RX) in different bands (TVWS, 2.6 GHz)
- To make first experiments in order to prepare the final experiments, demonstrations and the review.

2.1.2.1 **Overall setup**

The overall setup comprises:

- An eNodeB located in the EURECOM building, with capabilities in TVWS band (TDD duplexing mode) and 2.6 GHz (FDD duplexing mode).
- A terminal that is put in a car, as illustrated in Figure 3.

Figure 3 Equipped car for the experiments

2.1.2.2 **eNodeB specifications**

Table 1 illustrates the specifications for the eNodeB.

Table 1 Specifications for the eNodeB

TX transmitted power	+25 dBm (per path) in the TVWS (734 – 758 MHz) +30 dBm (per path) in the 2.6 GHz band
Noise figure	6 dB
Operated TX frequency band	TVWS : 734 – 758 MHz 2.6 GHz band: 2500 – 2570 MHz
Operated RX frequency band	TVWS : 734 – 758 MHz 2.6 GHz band: 2620 – 2690 MHz
Maximum input power	-30dBm
Maximum attenuation between antenna and PA-LNA module (due to the 20 m cables)	3 dB

2.1.2.3 **Terminal specifications for the chosen bands**

Table 2 illustrates the specifications for the terminal for the chosen bands.

Table 2 Specifications for the terminal

TX transmitted power	+20 dBm (per path) in the TVWS (734 – 758 MHz) + 20 dBm (per path) in the 2.6 GHz band
Noise figure	7 dB
Operated TX frequency band	TVWS : 400 – 790 MHz 2.6 GHz band: 2620 – 2690 MHz
Operated RX frequency band	TVWS : 400 – 790 MHz 2.6 GHz band: 2500 – 2570 MHz
Maximum input power	-30dBm

Figure 4 Equipped car on the road near Eurecom

2.1.2.4 **Coverage test**

The aim of this first experiment is to estimate the eNodeB coverage at 746 MHz and 2.6 GHz. The test is done around the EURECOM building, as illustrated in Figure 5.

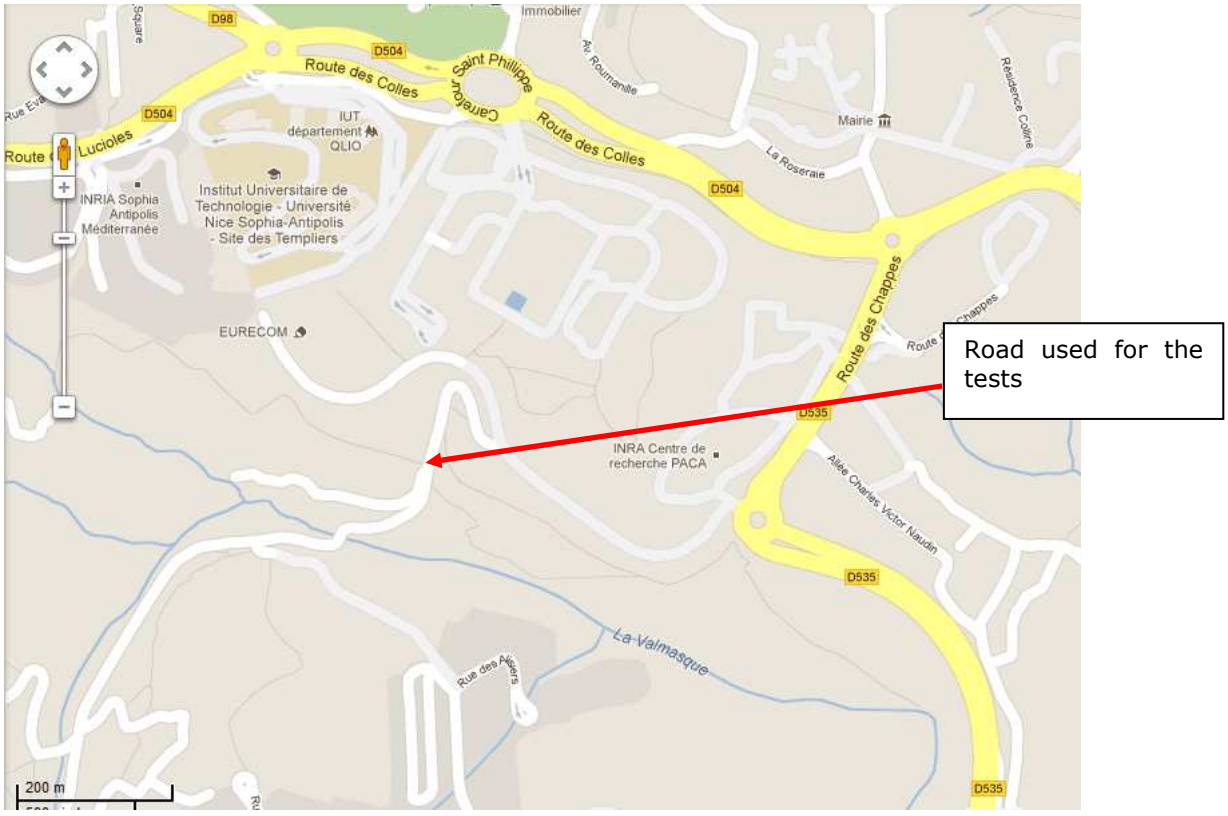


Figure 5 Location of the experimentations (map)

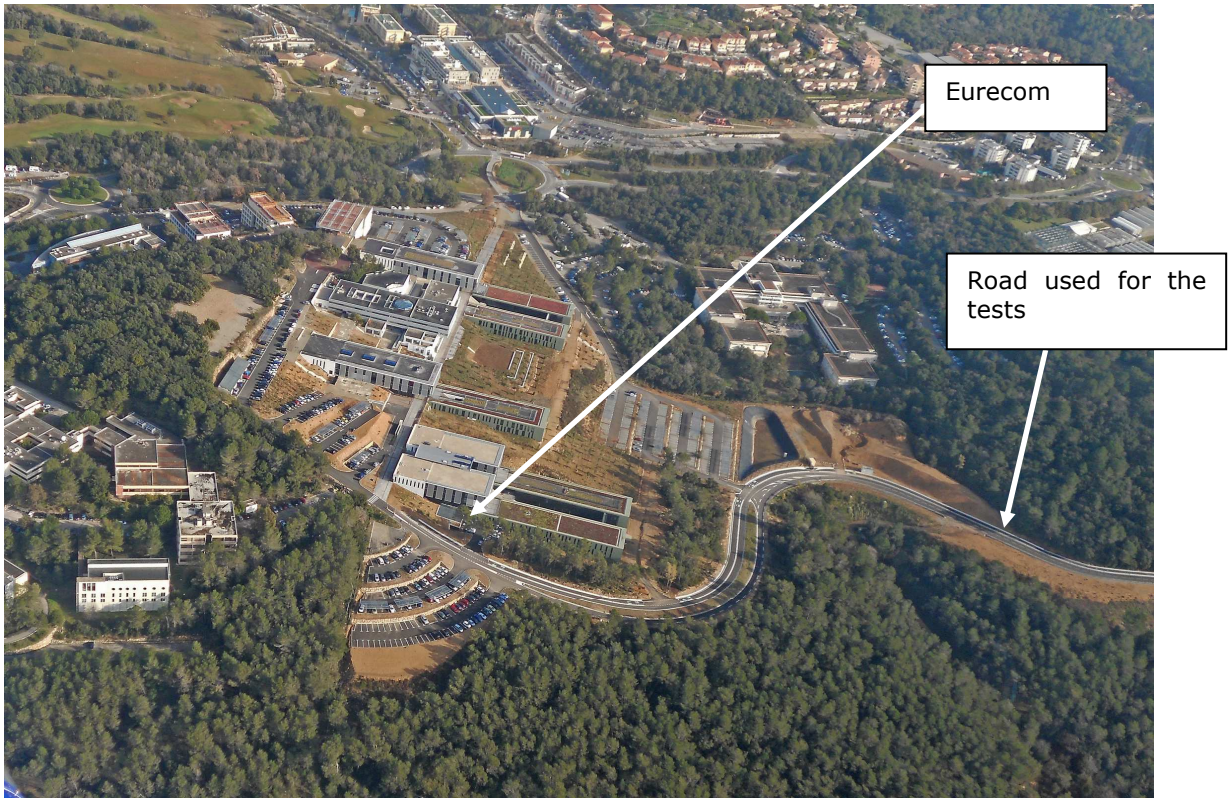


Figure 6 Location of the experimentations (photo)

For this test, the eNodeB transmits a sinusoid with a specified frequency, 746 MHz for the TVWS band, and 2.655 GHz for the 2.6 GHz band.

2.1.2.5 **2.6 GHz coverage**

Table 3illustrates the level received by the UE (Downlink) in various places of the road. The levels are given in dBm. The transmission is done by the eNodeB, the signal is a sinusoid at 2535 MHz, with a TX power of + 35 dBm. Only one antenna is used for both transmission and reception.

The measurements are done as follow:

- The eNodeB is transmitting a sinusoid with a calibrated power of +35 dBm (input of the antenna).
- The receiver is put in a car. The antenna is connected to a receiver with a calibrated gain of 25 dB at 2.6 GHz. The level is measured with a FSQ spectrum analyzer.

Table 3 2.6 GHz coverage measurements

	Measured level (FSQ input)	Ampli. gain(+25 dB)	Path loss (Pout-Prec)
1	-46	-71	106
2	-49,5	-74,5	109,5
3	-48	-73	108
4	-33	-58	93
5	-40	-65	100
6	-46	-71	106
7	-32	-57	92
8	-51	-76	111
9	-65	-90	125
10	-49	-74	109
11	-59	-84	119
12	-68	-93	128
13	-79	-104	139
14	-48	-73	108
15	-56,5	-81,5	116,5

One can see that the level of received signal by the terminal can vary from a very low level (-104 dBm) up to a very large one (-57 dBm). This test is therefore representative of many realistic situations of reception.

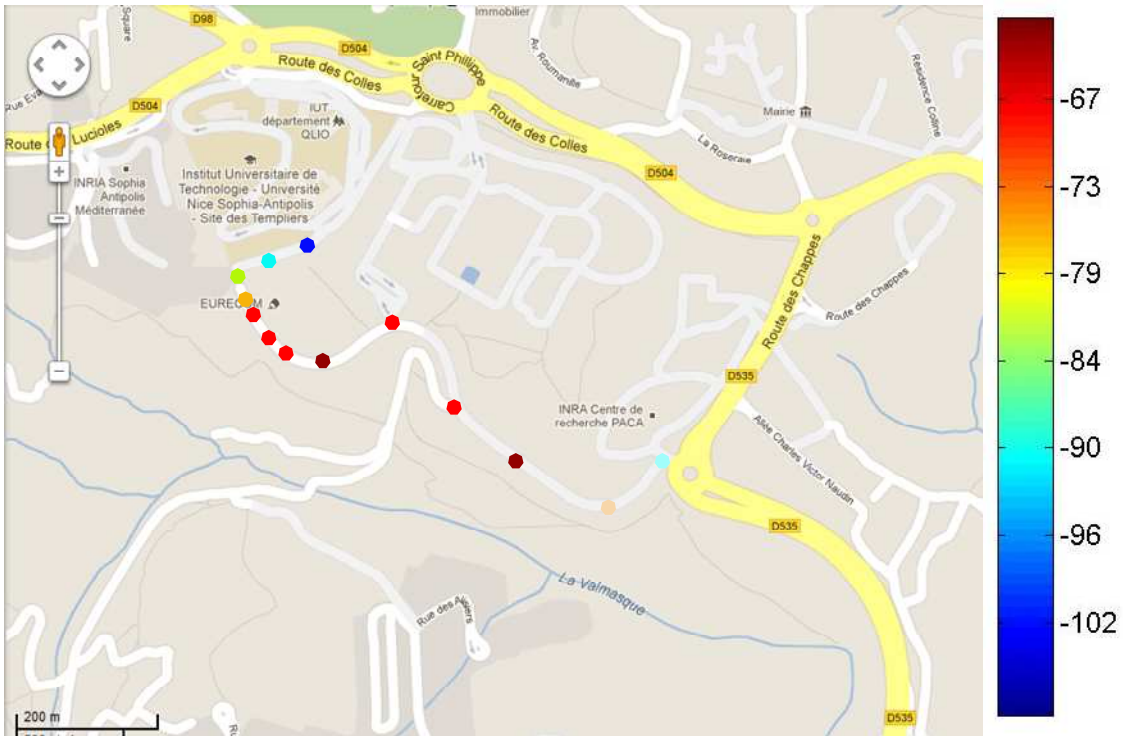


Figure 7 Level received by the UE in various places of the road (2.6 GHz).

2.1.2.6 **TVWS band coverage**

Table 4illustrates the level received by the UE (Downlink) in various places of the road. The levels are given in dBm. The transmission is done by the eNodeB, the signal is a sinusoid at 746 MHz, + 25 dBm. Only one antenna is used for both transmission and reception.

The measurements are done as follow:

- The eNodeB is transmitting a sinusoid with a calibrated power of +25 dBm (input of the antenna)
- The receiver is put in a car. The antenna is connected to a receiver with a calibrated gain of 21.3 dB at 746 MHz. The level is measured with a FSQ spectrum analyser.

Table 4 746 MHz coverage measurements

	Measured level (FSQ input)	Ampli. Gain (+21,3 dB)	Path loss (Pout-Prec)
1	-49,2	-70,5	95,5
2	-44	-65,3	90,3
3	-47	-68,3	93,3
4	-53	-74,3	99,3
5	-70	-91,3	116,3
6	-58	-79,3	104,3
7	-70	-91,3	116,3
8	-71	-92,3	117,3
9	-92	-113,3	138,3
10	-57,6	-78,9	103,9
11	-64	-85,3	110,3
12	-69	-90,3	115,3
13	-83	-104,3	129,3
14	-48	-69,3	94,3
15	-32	-53,3	78,3

One can see that the level of signal received by the terminal can vary from a very low level (-113 dBm) up to a very large one (-53.3 dBm). This test is therefore representative of many realistic situations of reception.

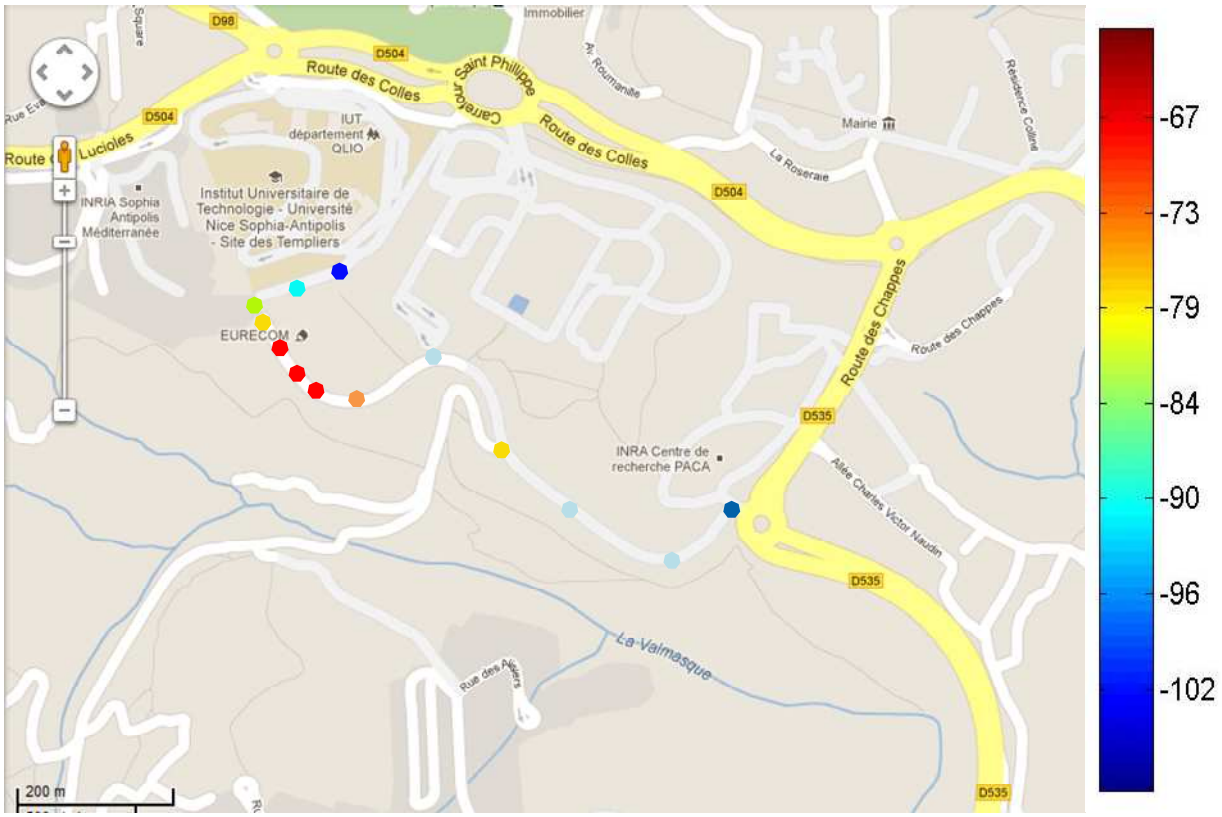


Figure 8 Level received by the UE in various places of the road (746 MHz)

2.1.2.7 **Dual band downlink and reception**

In this test, the eNodeB transmits a LTE signal (rel. 8 compliant)in the 2 bands, 2.6 GHz and TVWS. The details of the signals are the following:

- LTE Downlink signal
- BW = 5 MHz
- Modulation scheme for data : QAM-4
- TX power (2.6 GHz band) at 2535 MHz : +35 dBm
- TX power (TVWS band) at 476 MHz : +25 dBm

The 2 signals are received by the terminal. The test has been done in the laboratory (the laboratory is located in the room below the antennas, so the received signal is relatively high).

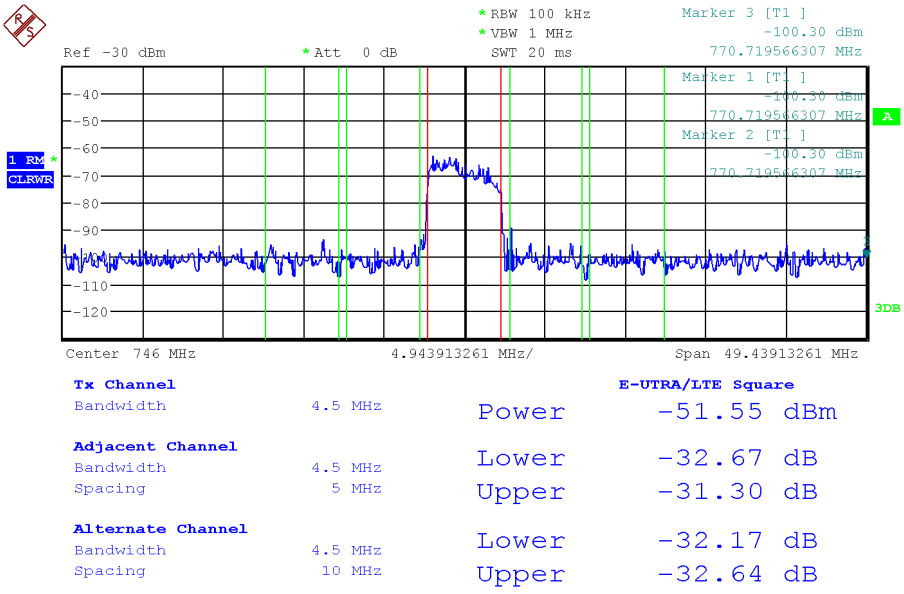


Figure 9 Downlink reception at 746 MHz

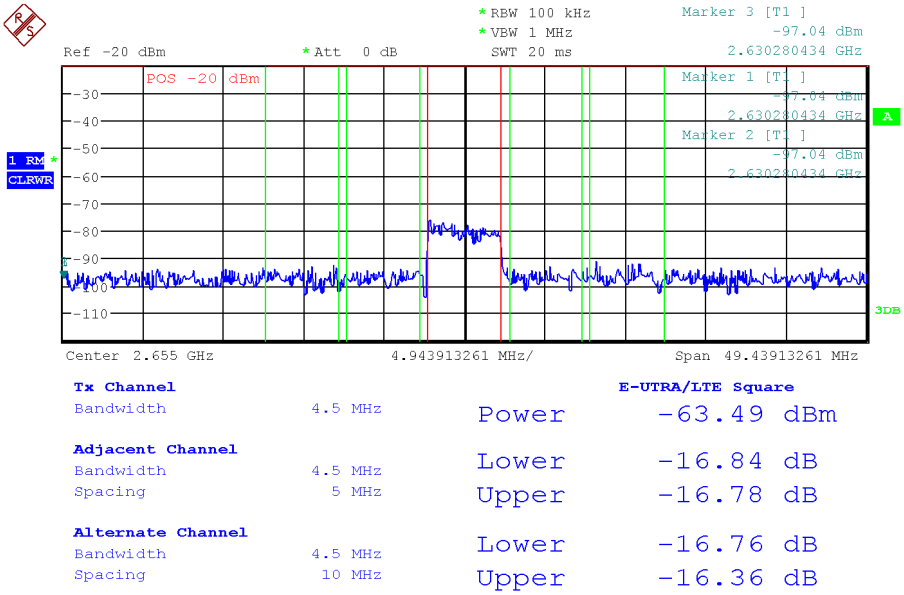


Figure 10 Downlink reception at 2655 MHz

2.1.2.8 **Primary users detection in the TVWS**

The scenario for the project includes the sensing of potential primary systems and the evacuation of the band. The goal of this test is to validate the emulation of a primary user for this scenario. In this test, we verify at first the occupancy of the TVWS band around the chosen frequency (746 MHz). The eNodeB receiver is enabled, and we analyse the received signal thanks to a spectrum analyser. The setup is the following:

- Centre frequency : 746 MHz
- Frequency span: 50 MHz
- Gain of the eNodeB receiver: 20 dB.

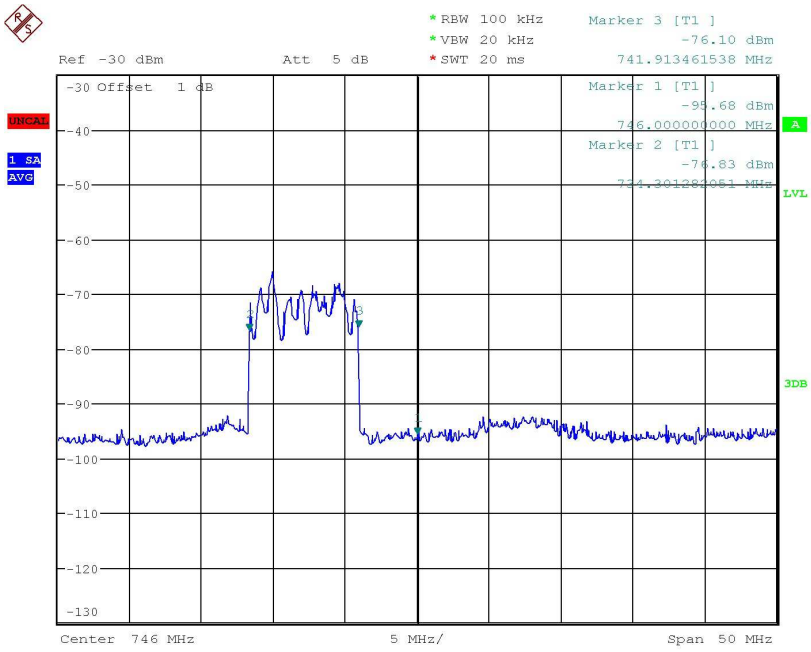


Figure 11 TVWS band occupancy

Clearly, the TVWS is occupied between 734.3 and 741.9MHz. The bandwidth of the signal is 7.6 MHz.

In a second step, we generate an emulated primary signal thanks to a signal generator. This test will allow us to make a dynamic demonstration thanks to a non-permanent primary signal. The following set up is used:

- Spectrum analyser : centre at 747 MHz, span of 100 MHz
- Emulated primary user : sinusoid, at 749 MHz, +12 dBm

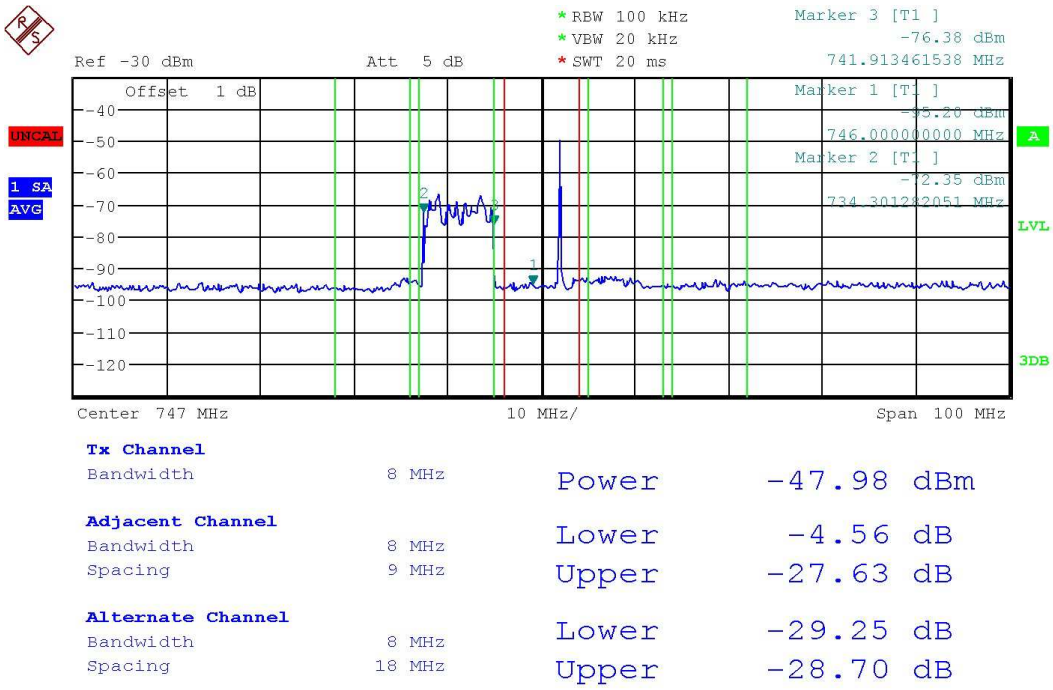


Figure 12 Emulation of a second primary user signal

The level of the emulated primary user is -68 dBm (-47.98 – Gain of the receiver). The test is successful, since we are able to put a signal in an arbitrary frequency with a significant level, in order to

stimulate the sensing/classification algorithms. One can notice that the actual primary signal is received with a level of – 72.56 dBm (-68 dBm – 4.56), which is also a high level.

2.1.2.9 **Uplink validation in the presence of an adjacent primary user**

The goal of this test is to verify the uplink in the case of a communication in the TVWS band. For this test, the setup is the following:

- Our experimental terminal based on ExpressMIMO2.
- The transmitted signal is at 746 MHz, LTE rel8., BW = 5 MHz, Modulation scheme for data: QAM-4, TX power = +12 dBm.
- The uplink is received by the eNodeB, a spectrum analyser is used at the output of the PA-LNA subsystem.

Figure 13and Figure 14illustrate the reception and the demodulation of the uplink signal.

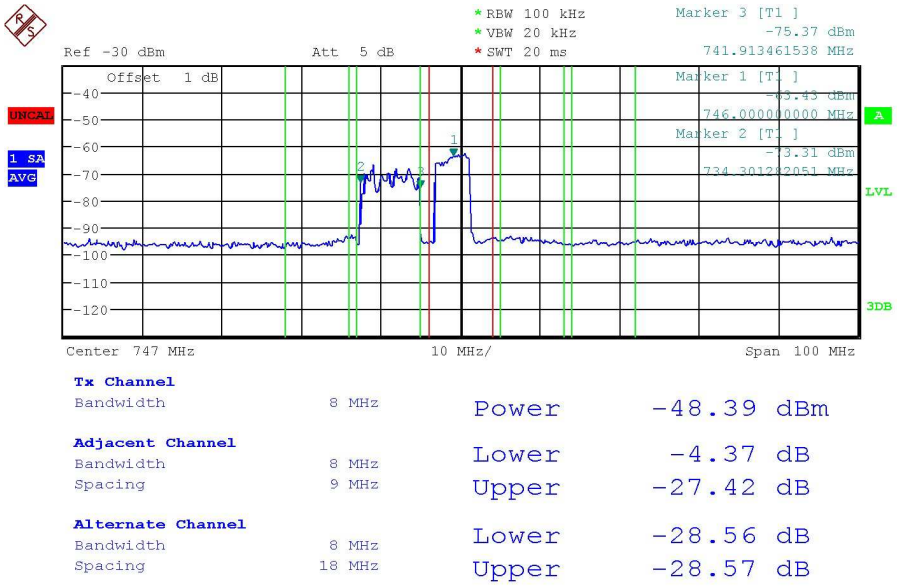


Figure 13 Reception of the uplink signal

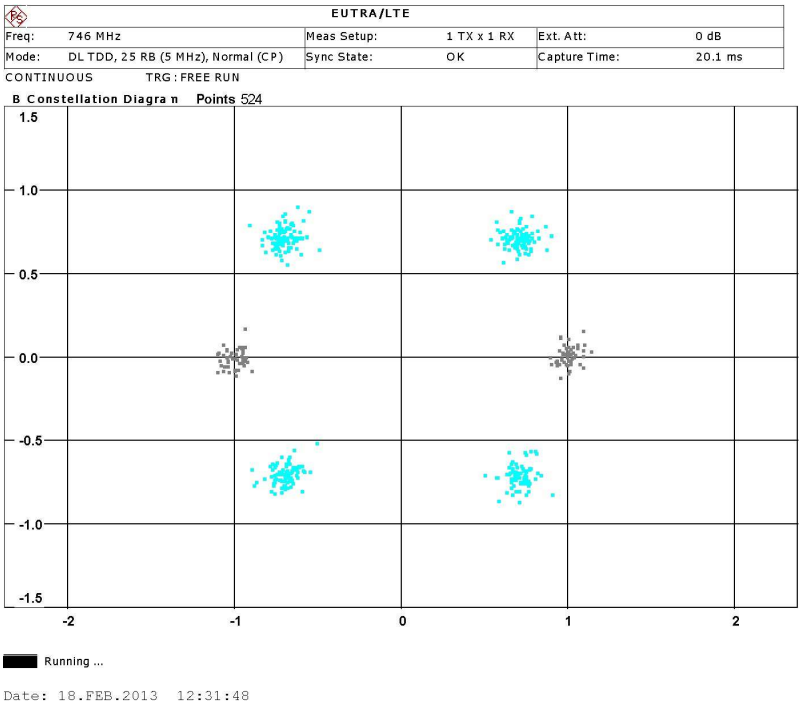


Figure 14 Demodulation of the uplink signal

As illustrated in the above figure, the LTE signal of interest is well received (blue points on the 4-state constellation).

2.1.3 Conclusions

In the previous sections, we have described:

- The set-up of the tests that have been conducted.
- The performed tests that allow evaluating the SHARING solution in a realistic environment.

In the previous stages of the work in SHARING, the tests have been done in the lab, or emulated. The performed tests will allow to experiment the SHARING solutions in a real environment. The next steps will consist of implementing the various use cases in the same environment, using the information given in the above sections.

2.2 Interference aware receiver for DL MU-MIMO CoMP (CEA)

2.2.1 Description

In D7.3 [1] and D7.2 [2], we have studied a CoMP downlink SL-MMSE receiver with interference rejection capabilities, following the theoretical studies in D3.2 [3].

Since the receiver is implemented at the UE, it was assumed that only two antennas were available at the receiver. Two transmit antennas were also assumed at both CoMP base stations. The SL-MMSE filter expression is given by

$$\boldsymbol{b}^H = \boldsymbol{b}_{SL-MMSE}{}^H = E_x \boldsymbol{g}_e^H \boldsymbol{R}_{\boldsymbol{y}}^{-1}$$

with E_x the transmit signal energy, $\boldsymbol{R}_{\boldsymbol{y}}$ the covariance matrix of the receive signal vector and $\boldsymbol{g}_e$ the effective channel composed of the combined effects of the precoding vectors and propagation channels between each of the two base stations involved in CoMP and the UE.

The fact that $\boldsymbol{R}_{\boldsymbol{y}}$ was of size 2x2 led to simplifications, since the inverse of a 2x2 matrix is quite easy to compute.

In this document, the hardware complexity was evaluated for a 4x4 matrix size (4 antennas both at the UE, which is a reasonable assumption for future terminals, and at the base stations). However, the methodology is generic and valid for any matrix size.

First of all, complex matrices were mapped on real ones, since decomposition algorithms such as QR apply to real matrices.

2.2.2 Complex to real matrix implementation

Matrix computation over complex numbers can be carried out over twice-sized real matrices. If A_c is a complex matrix and A_r its real form, we have:

$$A_r = \begin{bmatrix} Re\{A_c\} & -Im\{A_c\} \\ Im\{A_c\} & Re\{A_c\} \end{bmatrix}$$

Let's note f the function such that: $A_r = f(A_c)$. All operations (addition, multiplication, inverse) can be performed over complex or real form:

$$\begin{cases} f(A_c + B_c) = f(A_c) + f(B_c) = A_r + B_r \\ f(A_c.B_c) = f(A_c).f(B_c) = A_r.B_r \\ f\left({A_c}^{-1}\right) = \left(f(A_c)\right)^{-1} = {A_r}^{-1} \end{cases}$$

These properties lead to work over real matrices instead of complex matrices without loss of generality.

2.2.3 Solving SL-MMSE equation

The solution of the SL-MMSE equalisation filter is:

$$b^H = {R_y}^{-1}\boldsymbol{g}_e$$

Where b^H is a $(N_{Rx}, 1)$ matrix.

Two solutions will be studied:

- The first one has two steps. The first step consists in decomposing the R_y matrix in order to get simpler matrix (triangular matrix) to inverse. The chosen solution is the QR decomposition [4]of R_y : $R_y = QR$, with $Q^{-1} = Q^H$ and R an upper triangular matrix. The advantage of this decomposition is its computational stability with R condition number the same as that of R_y.

  In this case, the equation of the SL-MMSE is:

  $$b^H = (QR)^{-1}\boldsymbol{g}_e = R^{-1}Q^{-1}\boldsymbol{g}_e = R^{-1}Q^H\boldsymbol{g}_e$$

  The second step consists in solving the linear system $Rb^H = Q^H\boldsymbol{g}_e$to find b .

  Both algorithms have been described in RTL (Register Transfer level). Results are given in section 2.2.3.1.

- The second solution consists in directly inverting R_y without any assumption. This is described in section2.2.3.2.

2.2.3.1 QR matrix decomposition

The first step of the computation of the equalization filter consists in obtaining the QR decomposition of matrix$A = R_y$. The architecture is depicted inFigure 15. In order to reduce hardware complexity, this architecture is sequential, meaning that every sub-module is launched one after the other.

The module can process any square-sized matrix.

In Figure 15, the red arrows are used for data related to the reading process of the memories, and the blue ones are related to the writing process. The 2x2 matrix operations are started by the state machine. The starting and ending signals (inter-module synchronisation in Figure 15) enable to schedule the sub-modules.

The QR module also includes data stream control, it cannot receive data as long as the QR decomposition is not finished:

- "ready for data" output signal enables an external feeding module to send the matrix data that will be decomposed.
- "data request" input signal triggers the reading process of the matrices Q and R by another external module (in our case, the module which performs the linear system resolution).

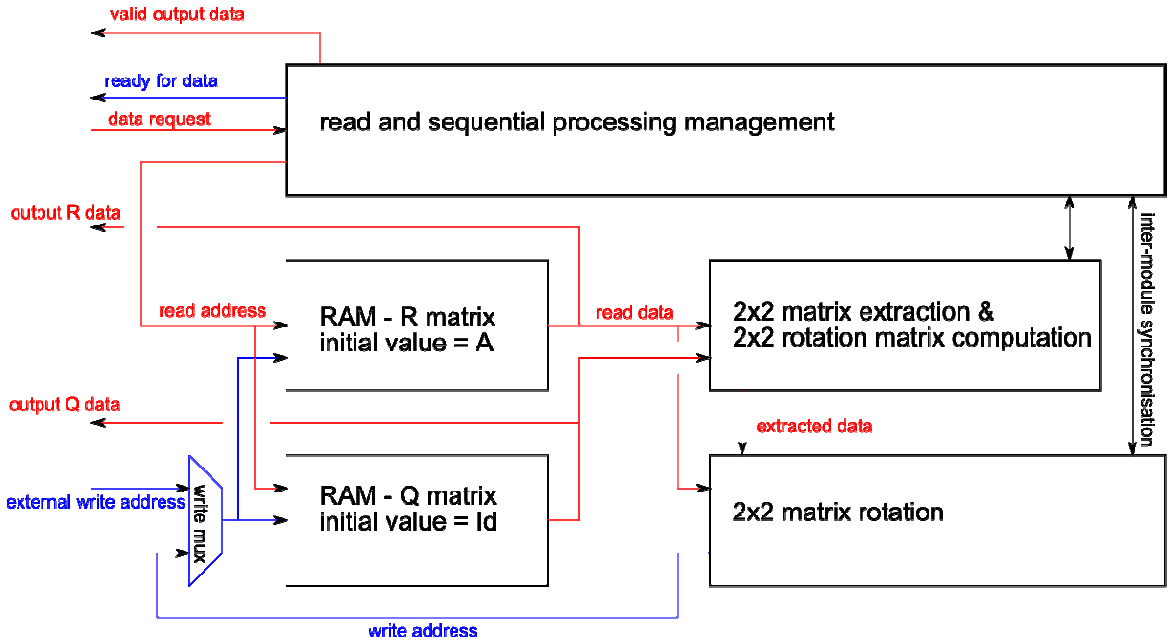


Figure 15 Architecture of the QR decomposition

The system loads two memories. At the beginning of the decomposition, the first one contains the matrix to decompose. The second one contains successively the cumulated rotation matrices. At the end of the processing the first memory contains R and the second one Q.

The architecture is then divided into three main parts. The "read and sequential processing management" manages the reading address of the two memories. At each step, once the data to process are read, the "2x2 matrix extraction" extracts the data to be rotated and computes the 2x2 rotation matrix. Finally the third part "2x2 matrix rotation" performs the rotation and writes the results into both memories. This process zeros sub-diagonal elements of the R Ram matrix until it becomes upper triangular.

Table 5gives the used resources with input/output real data dynamic 16 bits and (8,8) matrix size (equivalent to (4,4) complex matrix).

Table 5 Resource utilization of the QR decomposition algorithm

	Slice LUTs	Slice Registers	Block ram	DSP multipliers	Algorithm duration (in clock cycles)
(8,8) QR decomposition	5600	3800	0	8	486

Once Q and R are calculated, the second step consists in having a linear system resolution.

Linear system resolution

The linear system resolution is based on Jordan-Gauss method [4]. As the R matrix is upper triangular, there is no pivot to search.

Let's have the equation $RX = Y$ to solve with X the solution and Y the $(L,1)$ input. The extended matrix $\tilde{R} = [R \quad Y]$ is built. The dimensions are $(L, L+1)$. The method reduces the R part of $\tilde{R}$ to the identity matrix using linear operations over rows. At the end of the reduction, the Y part contains the solution X.

The linear operations include row division by the diagonal element and then rows combination in order to zero the non-diagonal elements. The architecture is depicted in Figure 16.

The stream control is identical to the one used in QR decomposition.

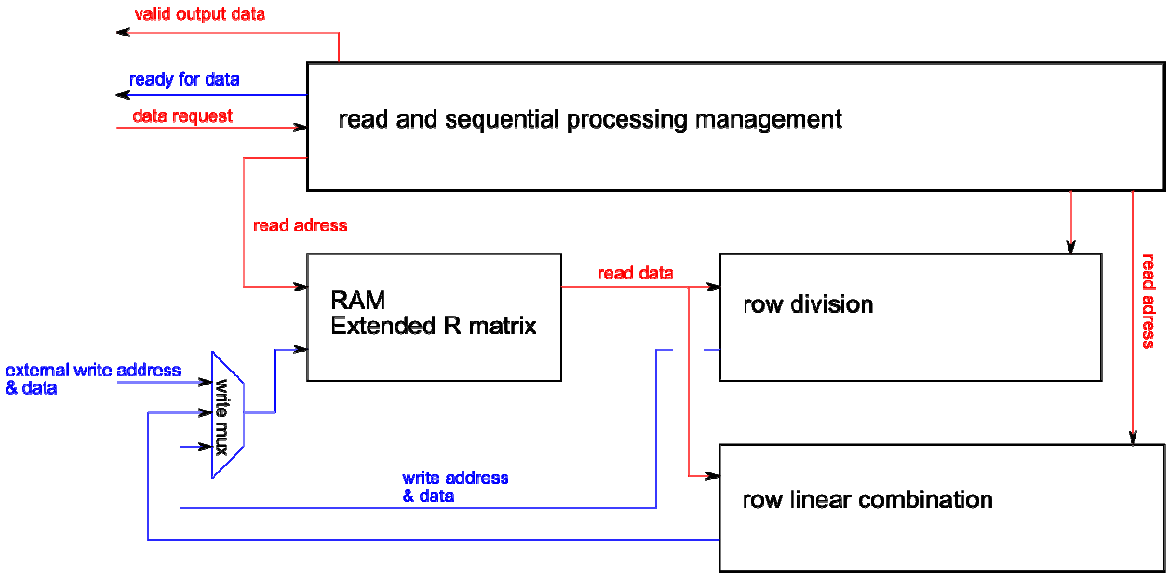


Figure 16 Architecture of the linear system resolution

Table 6gives the used resources with input/output real data dynamic 16 bits and (8,8) matrix size (equivalent to (4,4) complex matrix). The first line gives the figures for an arbitrary matrix whereas the second one gives them for an upper triangular matrix. As the operations are sequential, and both resolutions use the same operators, obviously, the complexity is the same. The difference is the number of clock cycles needed to get the result. The arbitrary matrix requires 1586 clock cycles (time when ready for data is equal to 0), whereas the upper matrix requires 1067 clock cycles. The gain is not two because the longest process is the row division, identical in both matrix processing.

Table 6 Resource utilization of the linear system solving

	Slice LUTs	Slice Registers	Block ram	DSP multipliers	Algorithm duration (in clock cycles)
Linear system (arbitrary input matrix)	11644	12621	2	4	1586
Linear system (triangular input matrix)	11634	12635	2	4	1067

2.2.3.2 **Matrix inversion**

The inversion of a matrix is based on the Jordan-Gauss method as described in the previous chapter.

Let's have the equation $AX = Y$ to solve with X the solution and Y the (L, L) input matrix. The extended matrix $\widetilde{R_y} = [R_y \quad Y]$ is built. The dimensions are $(L, 2L)$. The method reduces the R_y part of $\widetilde{R_y}$ to the identity matrix using linear operations over rows. At the end of the reduction, the Y part contains the solution $X = {R_y}^{-1}$.

The complexity and time duration are given in the Table 7.

Table 7 Resource utilization of matrix inversion

	Slice LUTs	Slice Registers	Block ram	DSP multipliers	Algorithm duration (in clock cycles)
Matrix inversion	11646	12623	2	4	2426

2.2.4 Conclusions

The comparison between the two solutions is given in Table 8.

The "QR + linear system solving" is more than 30% complex than direct matrix inversion. But the computational time is reduced by 60%.

According to the overall system complexity and timing requirements, the solution can be easily chosen.

Table 8 Solutions comparison

	Slice LUTs	Slice Registers	Block ram	DSP multipliers	Algorithm duration (in clock cycles)
QR + linear system solving	17244	16435	2	12	1553
Matrix inversion	11646	12623	2	4	2426

2.3 Carrier aggregation (CEA, TTI)

2.3.1 Introduction

This proof of concept (PoC) is related to carrier aggregation (CA) on the downlink for small cell scenarios. Two different hardware prototypes were jointly developed to support CA: the reconfigurable and flexible bandwidth RF front-end and the multi-band frequency agile antenna. Both demonstrators support the LTE Rel. 11[5] scenarios of intra-band CA band 7 and inter-band CA at band 20 and band 7.

The reconfigurable and flexible bandwidth RF front-end was developed to validate the analysis on the power amplifier (PA) requirements to support different CA configurations providing energy savings carried out in WP3[6][7]. A reconfigurable PA with different operating points is proposed to improve energy efficiency compared to conventional PA with single operating point. With the proposed solution, the output power at PA is adjusted depending on the number of component carriers (CCs) and CA mode using different operating points. Energy efficiency enhancement is tested in the hardware prototype for intra-band contiguous CA and intra-band non-contiguous CA comparing the performance with different operating points and single operating point. Details about its implementation and preliminary test results were presented in D7.3 [1].

The multi-band frequency agile antenna was developed in parallel with the RF front-end and optimized in terms of size and volume. The dual band antenna system is capable to adapt its frequency bandwidth according to the active CA configuration. This characteristic is achieved thanks to frequency agility and has led to a reduction of the instantaneous bandwidth of the antenna enabling its miniaturization. Details about its implementation and completed test results were presented in D7.3 [1].

2.3.2 Reconfigurable and flexible bandwidth RF front-end description

The reconfigurable and flexible bandwidth RF front-end to support CA was completely described in D7.3 [1]. The hardware prototype supports intra-band CA up to 3CCs in LTE band 7 (2620-2690 MHz) and inter-band CA in LTE band 20 (791-821 MHz) and LTE band 7 (2620-2690 MHz). Figure 17 presents the block diagram of the reconfigurable and flexible bandwidth RF front-end prototype.

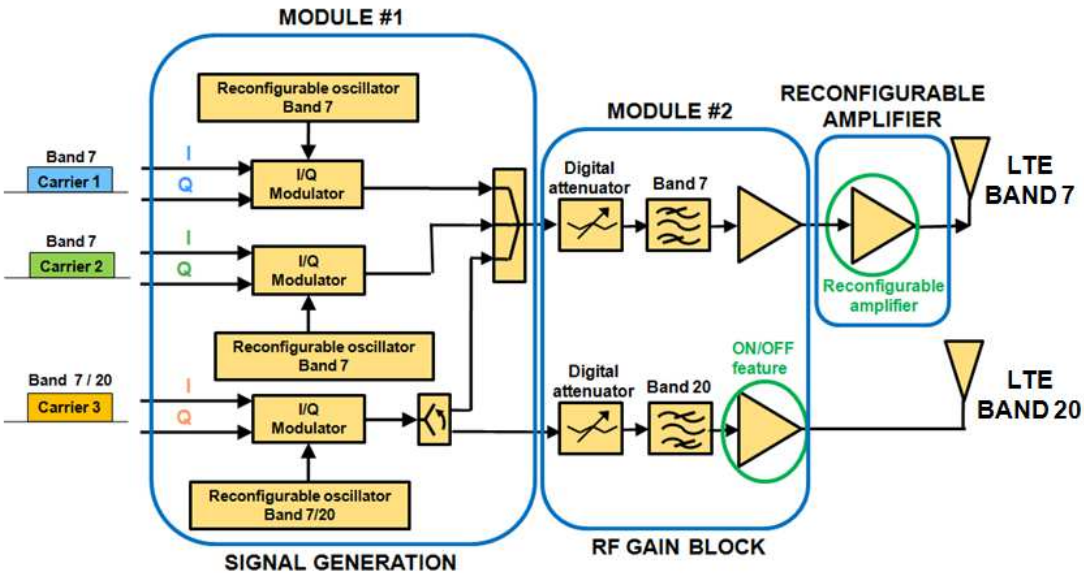


Figure 17 Block diagram of the reconfigurable and flexible bandwidth RF front-end prototype.

The hardware prototype is composed of three different modules: the signal generation module, the RF gain block module and the reconfigurable amplifier as depicted in Figure 17. The signal generation module provides different CA configurations from LTE baseband signals (E-UTRA test models) generated with Signal Studio software N7624B. The RF gain block module amplifies RF signals from the signal generation module. Through a digital attenuator the output power level is adjusted in order to test the reconfigurable amplifier performance for different CA configurations. Figure 18 shows the reconfigurable and flexible bandwidth RF front-end prototype.

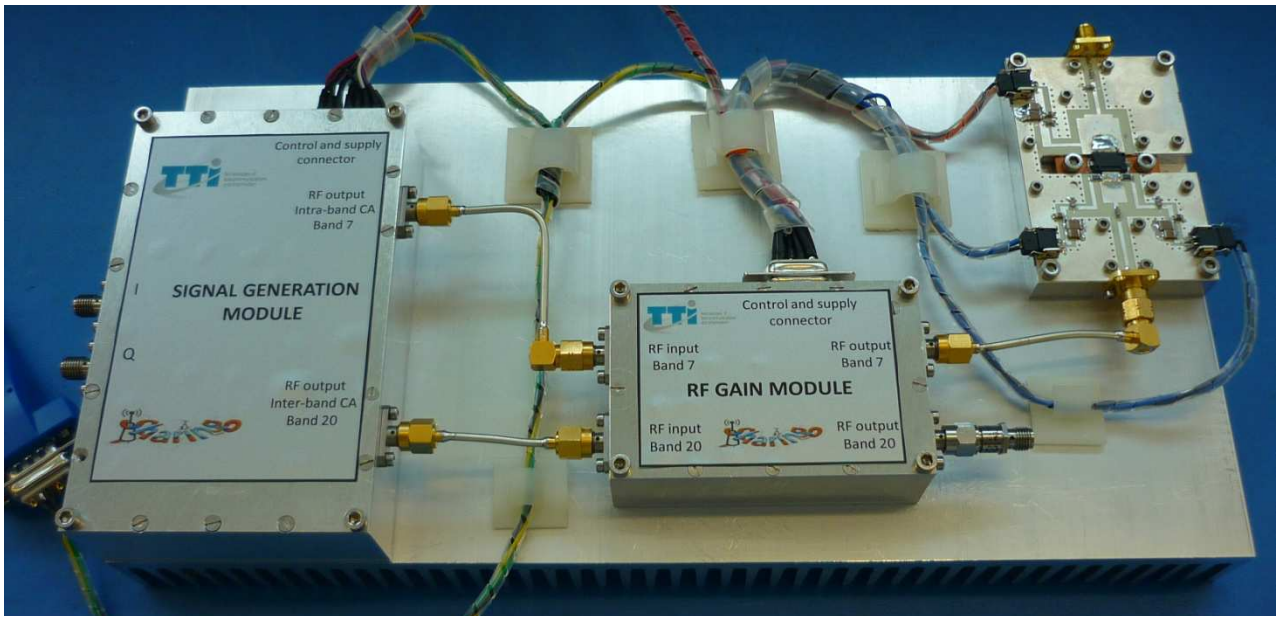


Figure 18 Reconfigurable and flexible bandwidth RF front-end prototype.

In order to operate the prototype, a console was prepared (Figure 19). This console runs in a laptop which connects with the prototype through RS-232 interface. The console is divided into four sections: Communication, Intra-band CA, Inter-band CA and Reconfigurable PA.

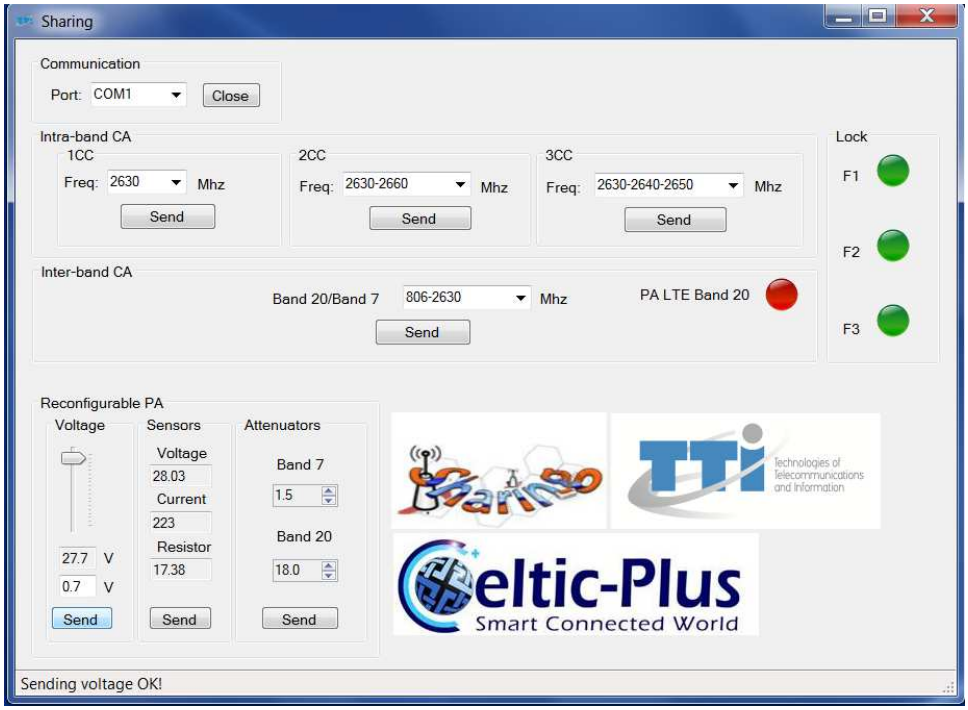


Figure 19 Console to operate the reconfigurable and flexible bandwidth RF front-end prototype.

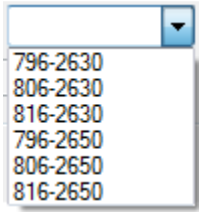
The communication section enables or disables the connection between the laptop and the prototype. The intra-band CA section builds up different intra-band contiguous and non-contiguous CA configurations. Into this section, there are three subsections to configure 1CC, 2CCs or 3CCs. For the validation, some frequency combinations into LTE band 7 were selected. Table 9 summarizes these possible frequency combinations for intra-band CA.

Table 9 Possible frequency combinations into LTE band 7 for intra-band CA.

1CC	2CCs	3CCs
2630 2640 2650 2660 2670 2680	2630-2640 2650-2660 2670-2680 2630-2650 2660-2680 2630-2660 2650-2680	2630-2640-2650 2660-2670-2680

The inter-band section is used to build up different inter-band CA configurations. Table 10 shows some possible frequency combinations for the validation. In this CA mode, the LTE band 20 PA should be switched on and there is a dedicated light which goes from red to green to indicate its operability.

Table 10 Possible frequency combinations into LTE band 20 and LTE band 7 for inter-band CA.



Finally, the reconfigurable PA section is dedicated to configure different operating points. The drain voltage applied to the reconfigurable PA is modified properly. Next to voltage subsection, there is the sensors subsection where the voltage and the current are measured through dedicated sensors. Furthermore, there is an attenuators subsection to adjust the gain in the RF gain block.

2.3.3 Reconfigurable and flexible bandwidth RF front-end validation

In D7.3 [1], the reconfigurable PA (AFT20S015) was tested at different operating points (from 28V to 14V drain voltage). It is observed that the higher is the drain voltage, thehigheristhe1dB compression point output power (P1dB). Therefore, the proposed reconfigurable solution can be adjusted depending on requirements demanded by CA configuration and the number of CCs to improve energy efficiency.

Different tests were done varying different parameters:

- CA configuration: intra-band contiguous, intra non-contiguousand inter-band.
- Number of CCs: 1CC, 2CCs and 3CCs.
- Frequency:
  - LTE band 7: 2630 MHz, 2640 MHz, 2650 MHz, 2660 MHz, 2670 MHz and 2680 MHz.
  - LTE band 20: 796 MHz, 806 MHz, 816 MHz.
- Operating point: 28V, 26V, 24V, 22V, 20V, 18V, 16V and 14V.

Figure 20 shows the setup to test the reconfigurable and flexible RF front-end prototype. The required lab equipment is two DC power supplies (+8V and +30V), one vector signal generator (N5182A) and one spectrum analyzer (N9010A).

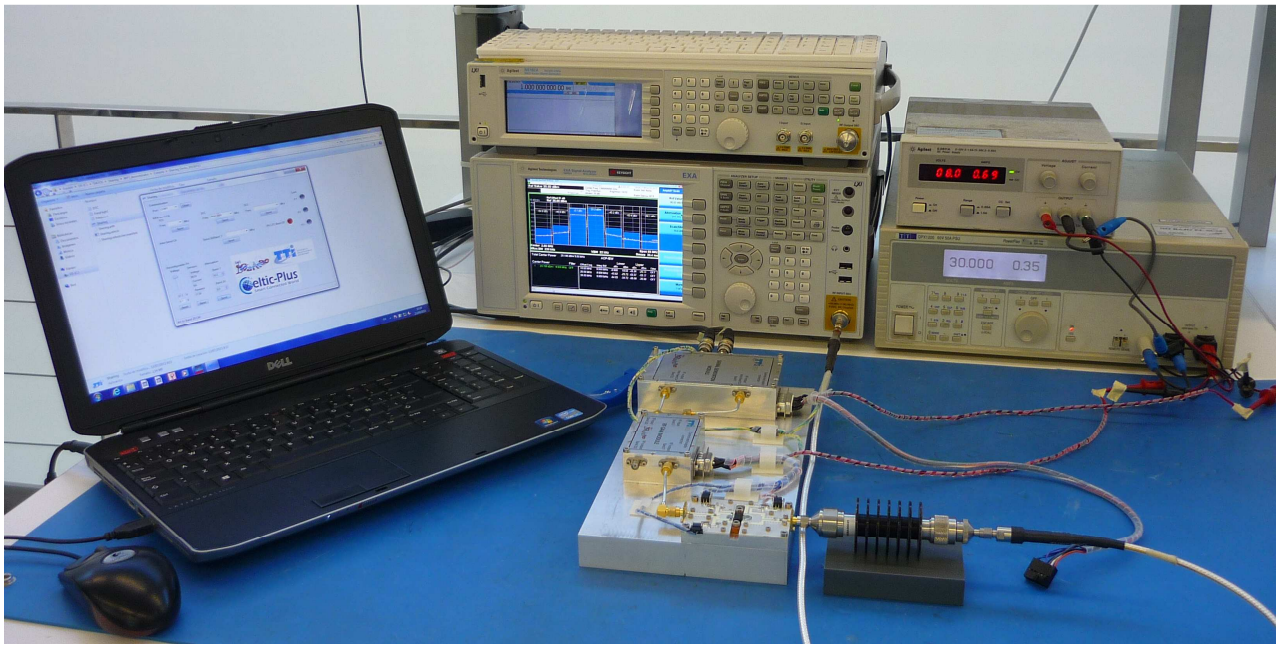
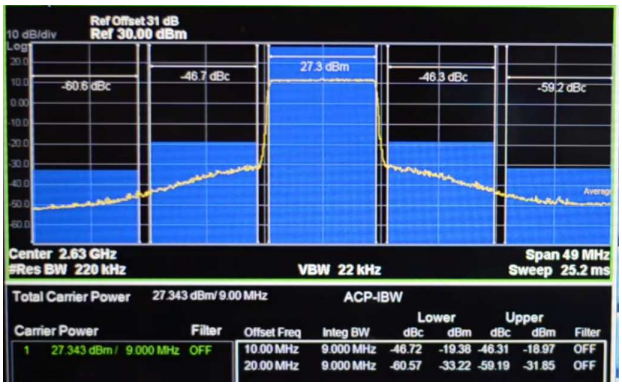
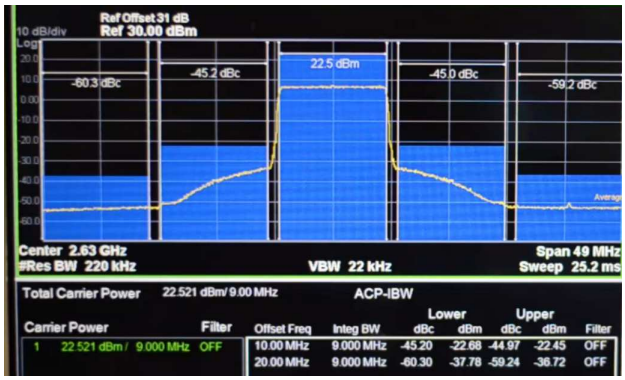


Figure 20 Test setup for the reconfigurable and flexible RF front-end prototype.

Using E-UTRA test signal, E-TM1.1, the average power to fulfil adjacent channel leakage ratio (ACLR) specification (at least -45dBc according to 3GPP standard) was tested for different CA configurations limited up to 3CCs. Figure 21 presents some examples of the measurement tests carried out in the prototype.

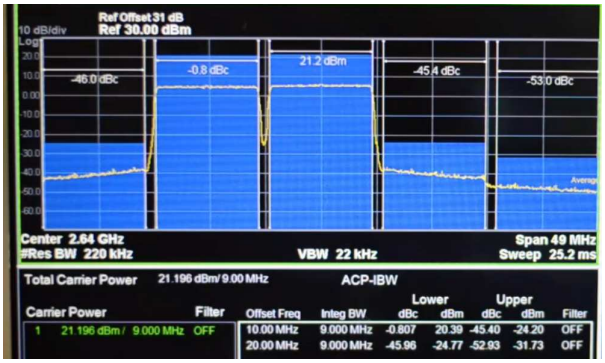


1CC at 2.63 GHz
28V operating point - 27.3 dBm average power

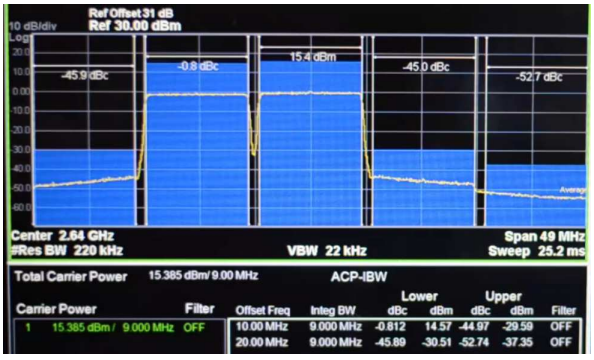


1CC at 2.63 GHz

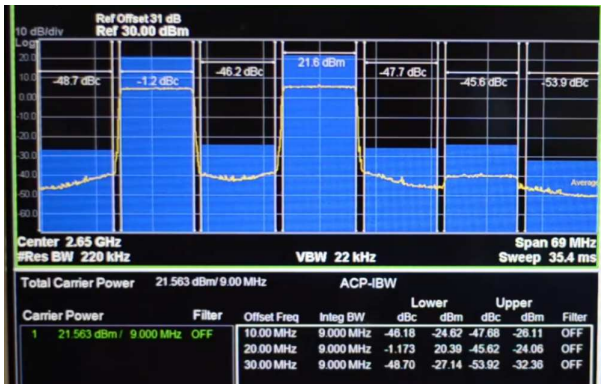
20V operating point – 22.5 dBm average power



2CCs contiguous at 2.63 GHz - 2.64 GHz
28V operating point – 21.2 dBm average power



2CCs contiguous at 2.63 GHz - 2.64 GHz
20V operating point – 15.4 dBm average power



2CCs non-contiguous at 2.63 GHz - 2.65 GHz

28V operating point – 21.6 dBm average power

3CCs contiguous at 2.63 GHz-2.64 GHz-2.65 GHz

28V operating point – 16.7 dBm average power

Figure 21 Some measurement tests carried out in the prototype.

Several tests are summarized in Table 11,Table 12, Table 13 and Table 14. Table 11 presents the average output power for 1CC at different operating points from 28V to 14V and at three frequencies in LTE band 7 (2.63 GHz, 2.65 GHz and 2.68 GHz). The average power shows the maximum output power for each operating point fulfilling ACLR specification.

Table 11 Maximum average power for 1CC at different operating points.

Operating point	Average power (dBm)		
	2.63 GHz	2.65 GHz	2.68 GHz
28V	27.3dBm	27 dBm	26.2 dBm
26V	26.5 dBm	25.6 dBm	25 dBm
24V	25.3dBm	24.3 dBm	23.7 dBm
22V	24.1dBm	22.9 dBm	22 dBm
20V	22.5dBm	21.3 dBm	20.6 dBm
18V	20.1dBm	19 dBm	18.8 dBm
16V	17.9dBm	17 dBm	16.2 dBm
14V	15.1dBm	14 dBm	13.6 dBm

At 2.63 GHz, the maximum average power is 27.3 dBm for 28V operating point and it reduces up to 15.1 dBm for 14V operating point. Depending on the required average power, it should select the lower operating point which delivers it because it presents better energy efficiency performance. Therefore, the proposed solution looks for the best operating point according to CA configuration and the number of CCs because different PA OBOs are required.

Table 12 shows the maximum average power for 2CCs in intra-band contiguous CA from 28V to 20V, and different frequency ranges into LTE band 7.

Table 12 Maximum average power for 2CCs at different operating points in intra-band contiguous CA.

Operating point	Average power (dBm)		
	2.63-2.64 GHz	2.65-2.66 GHz	2.67-2.68 GHz
28V	22.2dBm	20.5 dBm	19.6 dBm
26V	20.4dBm	19.2 dBm	15.8 dBm
24V	19.1dBm	18 dBm	16.6 dBm
22V	17.4dBm	16.2 dBm	15.2 dBm
20V	15.4dBm	13.9 dBm	13.1 dBm

Table 13 presents the results for 2CCs in intra-band non-contiguous CA with a gap between CCs equal to the CC bandwidth and Table 14 for a gap equal to twice CC bandwidth. The analysis was also done at different operating points from 28V to 20V and different frequency ranges into LTE band 7.

Table 13 Maximum average power for 2CCs at different operating points in intra-band non-contiguous CA (Gap = Bandwidth).

Operating point	Average power (dBm)	
	2.63-2.65 GHz	2.66-2.68 GHz
28V	21.3 dBm	20.2 dBm
26V	20.6 dBm	19.4 dBm
24V	19.2 dBm	17.7 dBm
22V	18 dBm	16.3 dBm
20V	16.2 dBm	14.2 dBm

Table 14 Maximum average power for 2CCs at different operating points in intra-band non-contiguous CA (Gap = 2*Bandwidth).

Operating point	Average power (dBm)	
	2.63-2.66 GHz	2.65-2.68 GHz
28V	22.7 dBm	21.8 dBm
26V	21.9 dBm	20.5 dBm
24V	20.6 dBm	19.1 dBm
22V	18.9 dBm	18 dBm
20V	17.1 dBm	15.6 dBm

Finally, the most restrictive CA configuration in terms of PA OBO for the prototype is 3CCs in intra-band contiguous CA with 15.9 dB OBO. Therefore this configuration should be configured with 28V operating point because provides the maximum power value. Table 15 shows the average power at two different frequency ranges into LTE band 7.Using 28V operating point the average power could be 16.7 dBm.

Table 15 Maximum average power for 3CCs in intra-band contiguous CA.

Operating point	Average power (dBm)	
	2.63-2.64-2.65 GHz	2.66-2.67-2.68 GHz
28V	16.7 dBm	15.8dBm

Regarding the energy efficiency evaluation in the proposed solution, the average power per CC in case of 3CCs in intra-band contiguous CA is considered as the reference because it is the most restrictive configuration. Therefore, the average power per CC is assumed about 17 dBm and it should identify the operating point for each CA configuration to reach around 17 dBm. Table 16 presents for each CA configuration the maximum average power using 28V operating point and evaluates the power-added efficiency (PAE) to bring around 17 dBm using 28V operating point or the optimized operating point.

Table 16 Energy efficiency evaluation for different CA configurations.

CA configuration	PA output back-off (dB)	Operating point (V)	Output power (dBm)	PAE (%)	PAE enhancement (%)
1CC	9.6 dB	28V	27.3 dBm	9.4%	---
		16V	17.9 dBm	2.8%	50%
		28V		1.4%	
2CCs non-contiguous (GAP = 2*Bandwidth)	11.8 dB	28V	22.7 dBm	3.9%	---
		20V	17.1 dBm	1.8%	39%
		28V		1.1%	
2CCs non-contiguous (GAP = Bandwidth)	12.6 dB	28V	21.6 dBm	3.3%	---
		21V	16.9 dBm	1.7%	35%
		28V		1.1%	
2CCs contiguous	13.4 dB	28V	21.2 dBm	3%	---
		22V	17.4 dBm	1.6%	25%
		28V		1.2%	
3CCs contiguous	15.9 dB	28V	16.7 dBm	1%	---

In case of 2CCs, there are different PA OBO requirements depending on CA configuration. Then 22V operating point is adequate for intra-band contiguous CA and 20-21V operating point for intra-band non-contiguous CA. At last it can reduce up to 16V operating point in case of 1CC.

For PAE enhancement evaluation, PAE is evaluated at 28V operating point considered as the conventional approach with single operating point and at optimized operating point according to CA configuration. For 2CCs in intra-band contiguous CA, PAE enhancement is around 25% and between 35-39% in intra-band non-contiguous CA. Achieving up to 50% for only 1CC.

Apart from that, inter-band CA was also evaluated. The prototype can also deliver 17 dBm in LTE band 20. Figure 22 shows measured output power at 806 MHz in inter-band CA configuration.

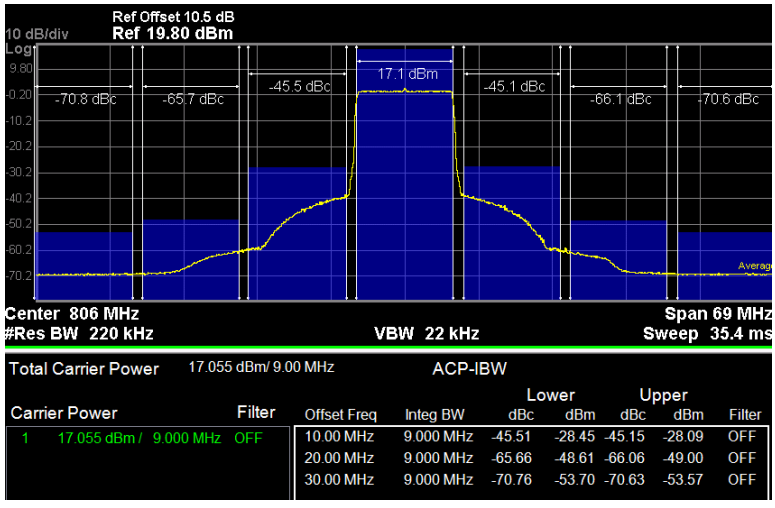


Figure 22 Measured output power at 806 MHz for inter-band CA

Furthermore, there is an LTE band 20 amplifier which is disabled during intra-band CA configurations and is enabled during inter-band CA configurations. This amplifier incorporates a fast power-up/power-

down function that provides a power saving mode, saving 1.5W related to its power consumption during intra-band CA. The total power consumption in the reconfigurable and flexible RF front-end is around 14-15W, so it is a considerable saving.

2.3.4 Carrier aggregation demonstrator validation

In the carrier aggregation demonstrator, the reconfigurable and flexible bandwidth RF front-end and the multi-band frequency agile antenna designed by CEA and described in [1], are combined as shown Figure 23. The interfaces between both prototypes are SMA connectors, one for each frequency band (LTE band 20 and LTE band 7). Therefore RF cables are required to connect both prototypes. A future version of the demonstrator would integrate the RF front-end on the back side of the antenna ground plane.

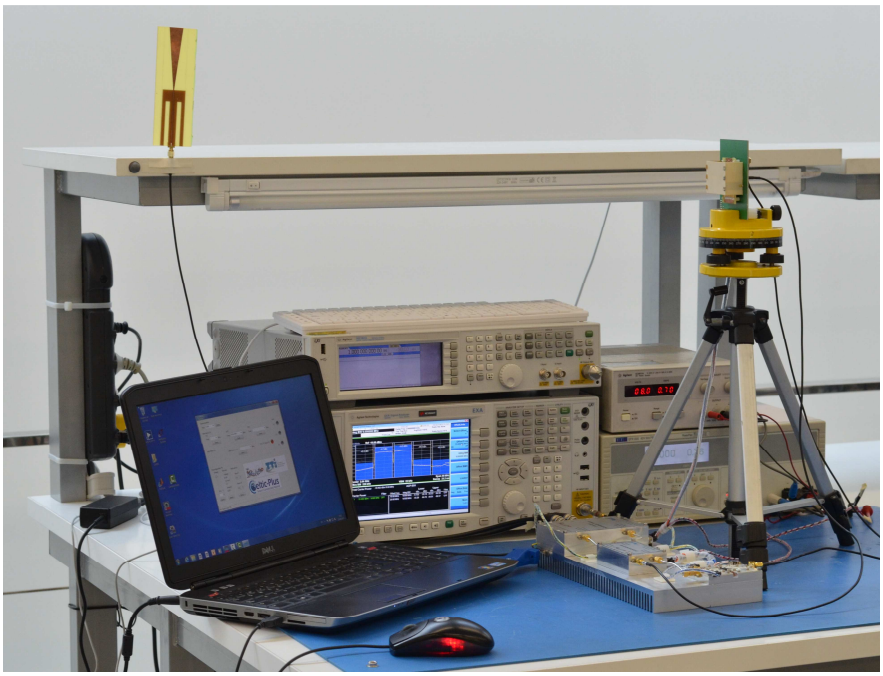


Figure 23 Carrier aggregation demonstrator setup

Furthermore, there is an auxiliary antenna which performs the antenna at user terminal. This auxiliary antenna is an omnidirectional antenna which operates at LTE band 20 and LTE band 7.

Figure 23 shows the CA demonstrator setup composed by the reconfigurable and flexible RF front-end, the multi-band frequency agile antenna, the auxiliary antenna and the required lab equipment (two power supplies, one vector signal generator (N5182A) and one spectrum analyzer (N9010A)). Moreover there is a console running in a laptop to control simultaneously the reconfigurable and flexible RF front-end and the multi-band frequency agile antenna.

Depending on the active CA configuration, the reconfigurable RF front-end is programmed with the appropriate frequencies. The LTE band 20 amplifier is only activated in inter-band CA configuration to save energy during intra-band CA. In the multi-band frequency agile antenna, the DTCs are also programmed to tune the antenna resonances properly. In LTE band 20, the frequency agile antenna has three different states that consist of one TX and one RX sub-channel both 10 MHz wide. Frequency agility is obtained through the use of two variable capacitors from Peregrine (PE6490x series). According to the selected frequency at LTE band 20 in the console, the required data is sent to the variable capacitors (DTCs) located in the antenna. These variable capacitors are controlled through the widely supported 3-wire (SPI compatible) interface. Table 17 presents DTC states for each channel in LTE band 20 antenna.

Table 17 DTC states for each channel in LTE band 20

	DTC1 (PE64909-HB-SEN1)		DTC2 (PE64904 – LB- SEN2)	
1 (796 – 837 MHz)	11	0x0B	21	0x15
2 (806 - 847 MHz)	5	0x05	9	0x09
3 (816 – 857 MHz)	1	0x01	2	0x02
	From 0 to 15	Hexa	From 0 to 31	Hexa

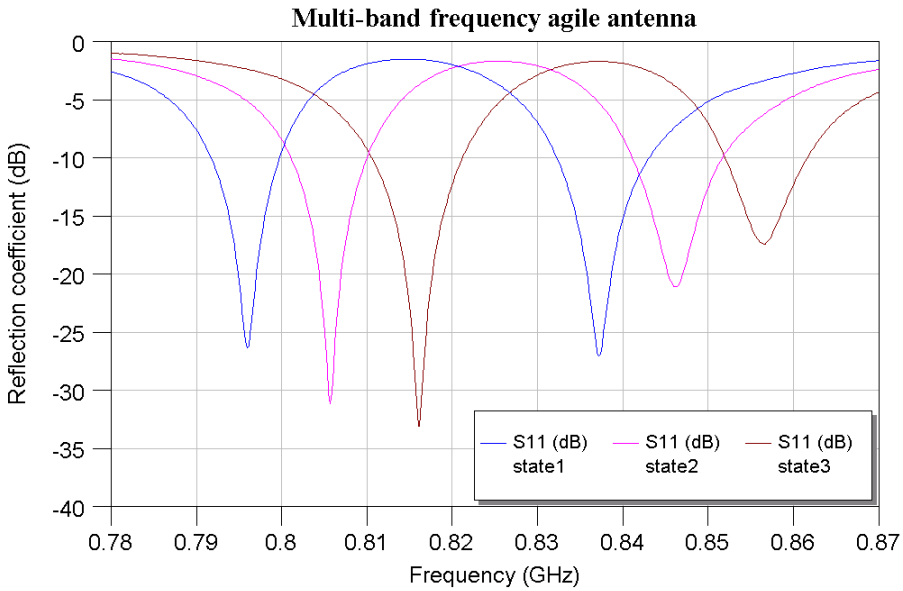


Figure 24 Reflection coefficient in the multi-band frequency agile antenna for the three states in LTE band 20.

To validate both prototypes, a radio link was performed among the small cell base station and the auxiliary antenna which emulates the user equipment antenna as shown Figure 23. Different CA configurations were tested and it checked that both prototypes work accurately. The tests were done in a lab environment and some interference appears in the measurements because mobile services operate in LTE band 20 and LTE band 7.Figure 25, Figure 26, Figure 27, Figure 28 and Figure 29 present some of CA tests performed in the CA demonstrator.

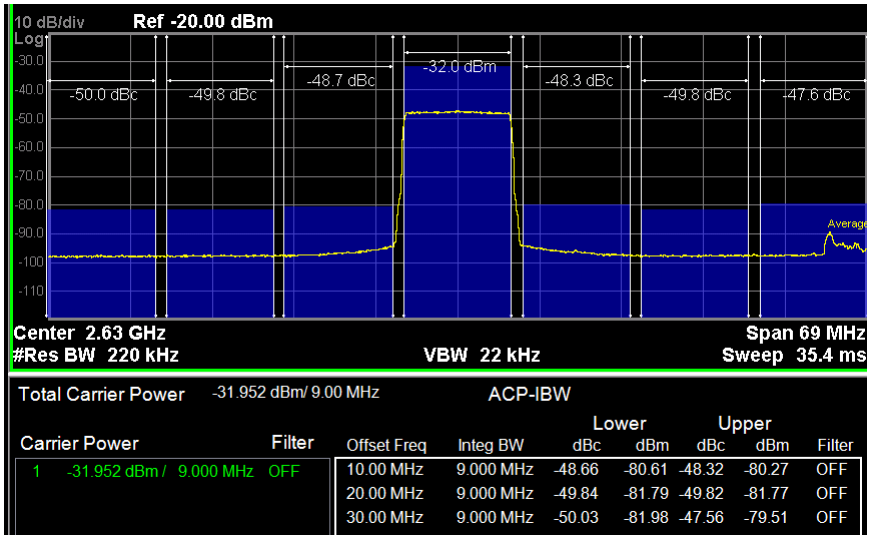


Figure 25 CA test with 1CC at 2.63 GHz in the CA demonstrator.

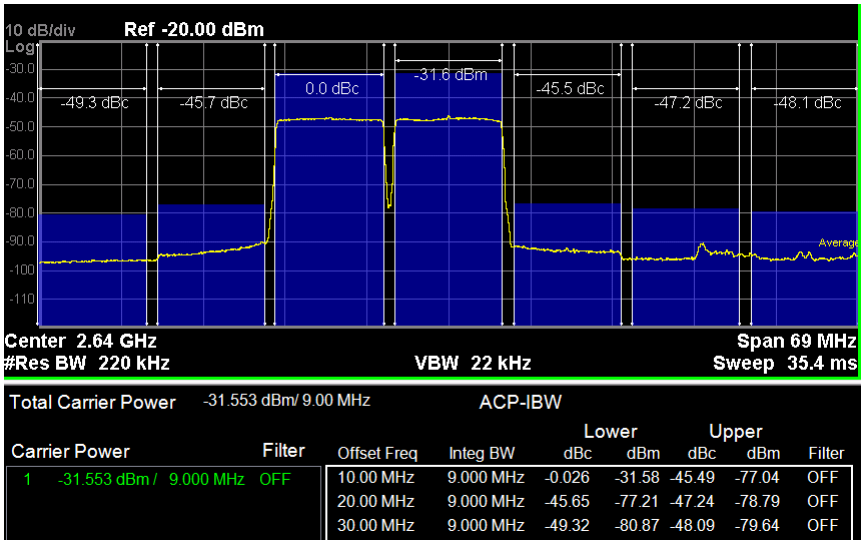


Figure 26 CA test with 2CCs at 2.63 GHz and 2.64 GHz in the CA demonstrator.

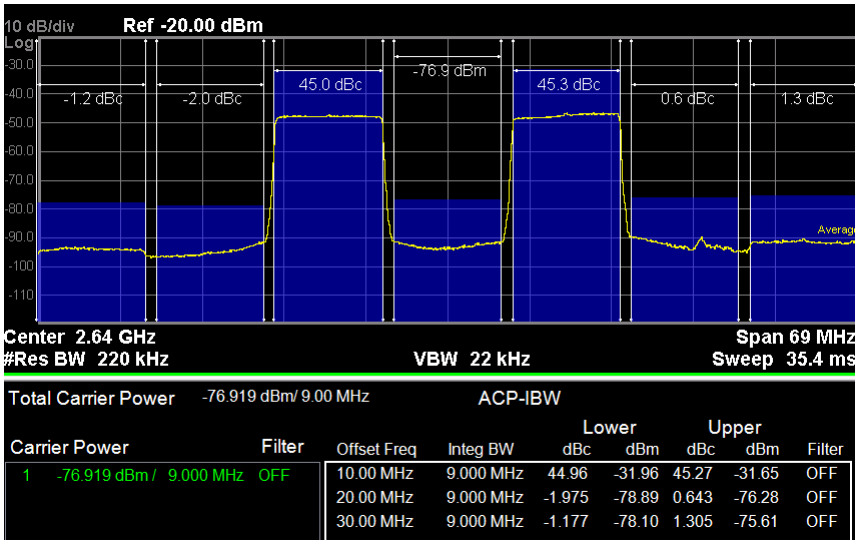


Figure 27 CA test with 2CCs at 2.63 GHz and 2.65 GHz in the CA demonstrator.

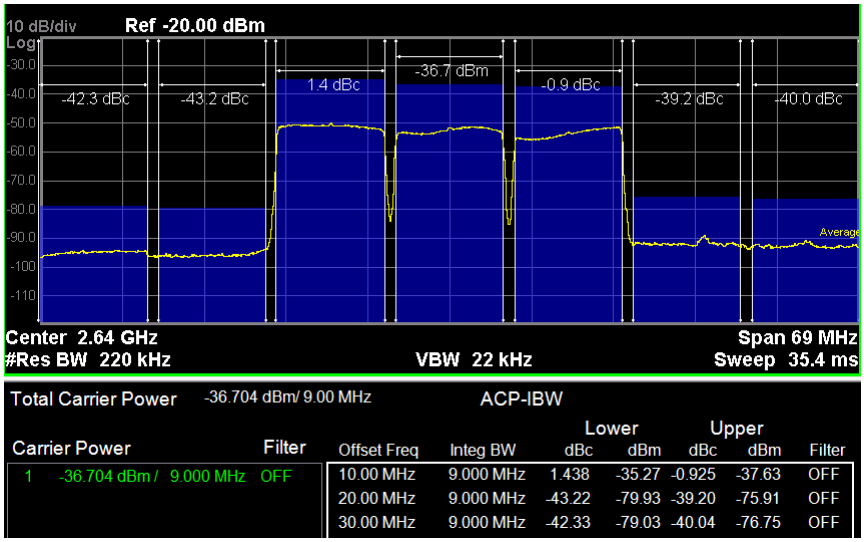


Figure 28 CA test with 3CCs at 2.63 GHz, 2.64 GHz and 2.65 GHz in the CA demonstrator.

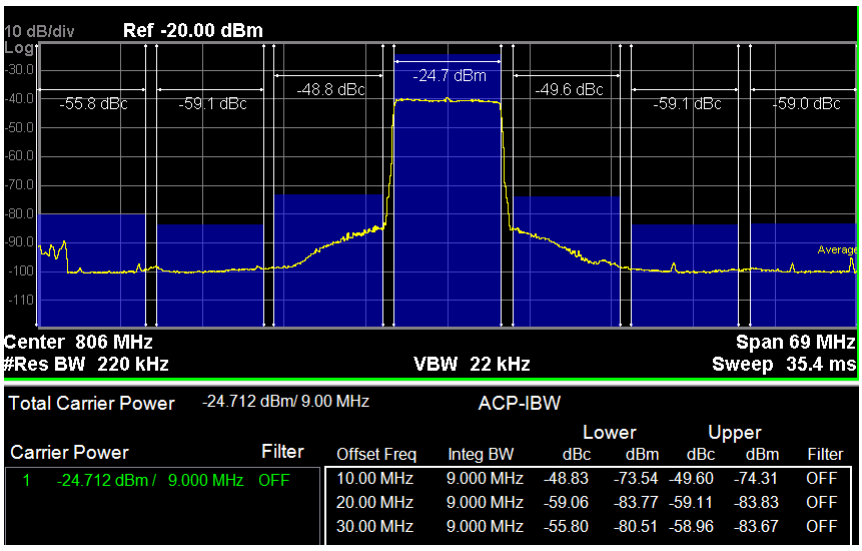


Figure 29 CA test with 1CC at 806 MHz in the CA demonstrator.

Additionally, a video was recorded summarizing the measurements carried out in the CA demonstrator.

2.4 Wi-Fi offloading (AVEA)

2.4.1 Description

This proof-of-concept is related to the integrated Wi-Fi offloading platform in mobile operator (MO) networks. The developed platform called SHARING is a connectivity management platform that uses a multiple attribute decision making (MADM) algorithm for efficient Wi-Fi Offloading in heterogeneous wireless networks. The proposed platform collects several terminals and network level attributes via infrastructure and client APIs and decides on the best network access technology (i.e. 3GPP and non-3GPP) to connect to for requested users.

The SHARING platform is compatible with two different operational modes. At first, it is with an integrated Wi-Fi and LTE operator's platform, where a single operator is responsible for both Wi-Fi and LTE infrastructure. Secondly, it can work with independent Wi-Fi and LTE operators where the two operators are communicating with SHARING platform in order to perform smart offloading. In this implementation, we assume that the SHARING platform is deployed by an operator providing Wi-Fi and LTE integrated services.

The details on the requirements, implementation, interfaces and integration of the SHARING platform were provided in SHARING Deliverable D7.3 [1] and the utilized MADM algorithm was described in SHARING Deliverable D4.3[8]. In the following sections we present the validation results and provide conclusions.

2.4.2 Validation Results

We present two different validation results via experimentation. In the first one, network selection experiment for a mobile SHARING Client is performed. In the second one, experiments to analyse the sensitivity of attribute weights for a static SHARING client are performed. The experimental set-up is provided in Figure 30. In the experimental set-up there is one WLAN AP A, one eNodeB, one mobile phone running a SHARING client application and one PC to configure the SHARING server deployed at Amazon Web Services. The details of attributes to be used in validations were previously presented in D4.3 [8] and D7.3 [1].

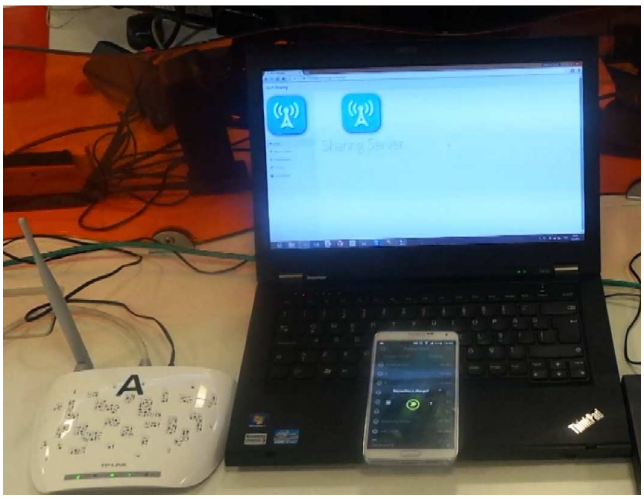


Figure 30 Experimental Set-up

2.4.2.1 Network Selection Experiment

The SHARING platform ensures that the mobile terminal is connected to the best available network based on the observed attributes. In order to provide a simplified demonstration of the performance, two attributes, RSSI (s_1) and number of connected users (s_4), are set as the most important attributes, i.e. $w_1 \approx 0.5$ and $w_4 \approx 0.5$. The candidate network set consists of two wireless networks, i.e. $p = 2$ and $E = \{WLAN, LTE\}$. Both candidate networks are previously registered to the SHARING server by Registration API. SHARING client is moved back and forth between different distances to WLAN AP A and eNodeB and the total number of connected users is varied to simulate a dynamic heterogeneous network environment.

The values of observed attributes, RSSI and number of connected users, and output of the experiment which is the selected network are presented in Figure 31. The experiment covers around 450 seconds of real-time observations and ST algorithm (as defined in D4.3 [8]) is used in the SHARING server. Initially, there are 6 users connected to eNodeB, 3 users connected to WLAN AP and the RSSI values for the LTE network are higher. Based on this initial setting, the SHARING server decides for SHARING client to connect to WLAN network at the beginning due to lower number of connected users although LTE network has higher RSSI values. During the experiment, around time 470 seconds, number of users connected to eNodeB drops to 4, and the SHARING server selects LTE as the best available network, thus the mobile terminal switches to LTE. Later on, around time 545 seconds, RSSI value of WLAN AP suddenly surpasses that of LTE, and SHARING client is requested to switch to WLAN. Then, around time 665 seconds, the number of users connected to WLAN AP experiences a sudden increase, and SHARING client switches to LTE. Then, until the end of the experiment, the mobile terminal stays connected to LTE despite larger RSSI values of WLAN, since number of connected users becomes the dominant factor in this region.

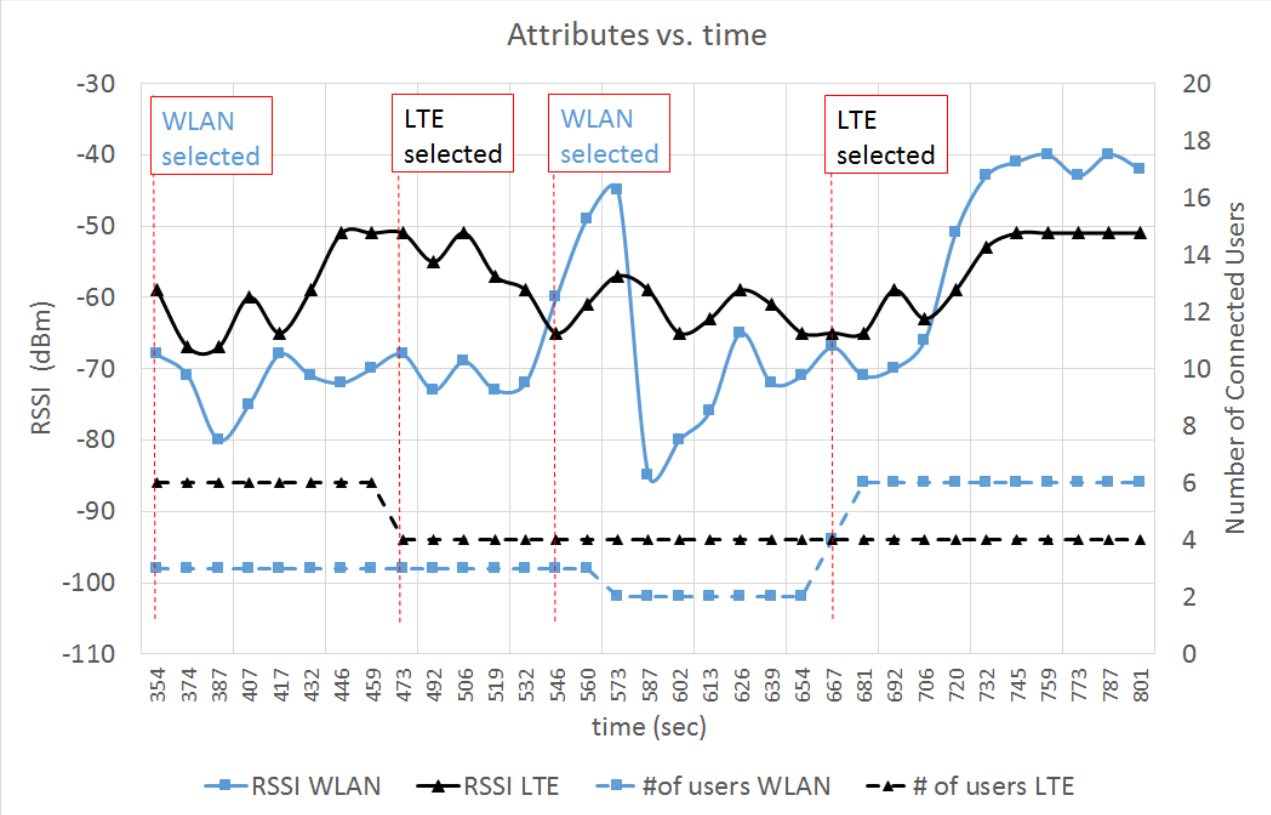


Figure 31 Network selection experiment results

2.4.2.2 **Sensitivity Analysis Experiment**

For the sensitivity analysis experiment, the experimental set-up is similar to the experiment performed in previous section as given in Figure 30. However, on the contrary to the network selection experiment, the SHARING client is now static during the experiment in order to test the sensitivity of the attribute weight w_4, i.e. the weight of the number of connected users attribute.

In Figure 32, the experiment results are given, where the average RSSI values of WLAN AP A and eNodeB are represented with dotted blue and red lines, respectively. In this set-up, since initially SHARING client is attached to WLAN AP A, we want to identify the sensitivity of increasing connected users to WLAN AP A before it switches to eNodeB for different values of w_4 weight values. In this type of experiment, number of connected users to eNodeB is 5 and number of connected users to WLAN AP A is varied from 1 to 100 inside SHARING server. For our experiments the value of w_4 are varied from 0.1 to 1.0 with 0.1 increments, while other attributes are assigned equal values after subtracting w_4 from 1.

Figure 32 shows average number of users at WLAN AP A before SHARING client switches to eNodeB as the attribute weight of number of users increases (the solid black line, represented by N_{WLAN}^{LTE}). As observed from the results in Figure 32, the increase in w_4 results in lower N_{WLAN}^{LTE}. For example, when $w_4 = 0.1$, N_{WLAN}^{LTE} becomes 83 and when $w_4 = 0.9$, $N_{WLAN}^{LTE} = 6.2$. The results in Figure 32 also illustrate that when w_4 is greater than 0.6, as the number users at WLAN AP A becomes marginally higher than eNodeB (which is fixed to 5), SHARING client hands-off from WLAN AP A to eNodeB. This means that for $w_4 < 0.5$, number of users connected to WLAN AP A has to be significantly larger than the number of users connected to eNodeB for SHARING client to perform hand-off. In addition, when $w_4 < 0.5$, in some cases of the experiment, SHARING client did not switch to eNodeB even if the number of connected users in WLAN AP A became very large, since the experiment results present only the cases when there is a hand-off. Note also that, this is the main reason behind the fall in the value of the average RSSI of WLAN AP A for $w_4 < 0.5$ since the number of handovers only occurs in cases when WLAN AP A RSSI level becomes lower. This result also indicates that when RSSI difference between the access technologies is large the balancing value for w_4 should be held between 0.5 and 0.6.

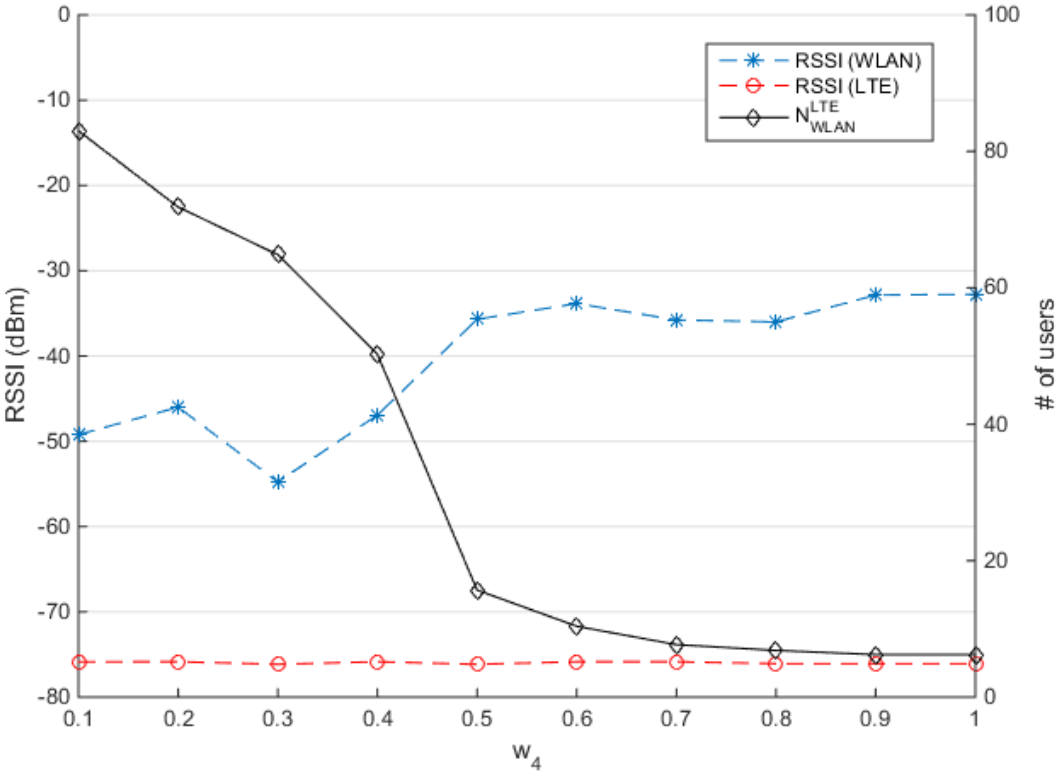


Figure 32 Sensitivity analysis experiment results

2.4.3 Conclusions

We have presented a proof-of-concept connectivity management platform for mobile operators which enables smart offloading decisions to service provider's users. The analysis, design and integration aspects as well as definitions for interfaces with infrastructure providers have been discussed. The proposed platform is designed as a client-server architecture where the mobile operator deploys a centralized connectivity management server called SHARING server which is running a MADM algorithm called TOPSIS. The best connectivity decisions computed by the SHARING server are fed back into the mobile terminal running the SHARING client application for enhanced user connectivity experience. Multi-user extension of TOPSIS algorithms is also proposed. A simplified demonstration of the performance of the platform as well as simulation results of the proposed multi-user extensions of TOPSIS algorithms are provided where the results demonstrate system level optimization. Experimental evaluations for the sensitivity of the weights of the MADM algorithm provides guide for operators on adapting Wi-Fi offloading platforms into their network infrastructures.

2.5 Reconfigurable and low power APT-VDF filter implementation based on dynamic partial reconfiguration in FPGAs (SUP)

2.5.1 Description

This proof-of-concept is related to the implementation of a variable digital filter (VDF) with unabridged control over cutoff frequency, using FPGA dynamic partial reconfiguration. The implemented filter is an all-pass transformation (APT) based variable digital filter which is obtained by replacing each unit delay of the digital filter by a first-order all-pass structure as depicted in Figure 33. This filter can provide variable frequency response with unabridged control over cut-off frequency. The advantage of the APT-VDF filter is that it allows fine control over cut-off frequency without updating the filter coefficients or structure. The first order all-pass filter structure is shown in Figure 34.

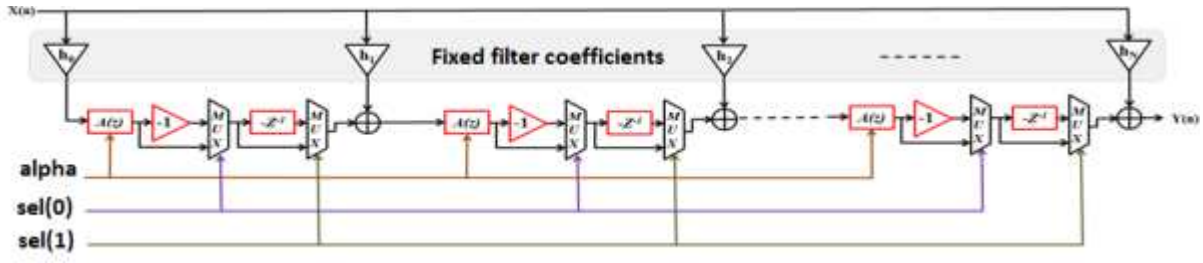


Figure 33 APT-based VDF filter architecture

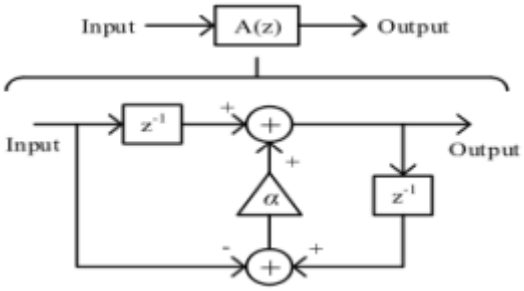


Figure 34 First order all-pass filter hardware implementation structure.

If$H(z)$ and$A(z)$ are the z-domain transfer functions of the prototype filter and the first order all-pass filter, respectively, the z-domain transfer function $G(z)$ of the APT-VDF filter is given in Table 18. The parameter *Sel* is a 2-bits signal used to select which filter type will be used (Lowpass, Bandpass, Highpass, Bandpass).

Table 18 APT-VDF filter response versus parameter *Sel*

$A(z)$	$H(z)$: Lowpass	**Sel(1)**	**Sel(0)**	$G(z)$
$\frac{-\propto +z^{-1}}{1-\propto z^{-1}}$; $\lvert\propto\rvert < 1$	$\sum_{0\le i\le N} h_i z^{-i}$	**0**	**0**	$G(z) = H(A(z))$: variable Lowpass
$\frac{-\propto +z^{-1}}{1-\propto z^{-1}}$; $\lvert\propto\rvert < 1$	$\sum_{0\le i\le N} h_i z^{-i}$	**1**	**0**	$G(z) = H(-z^{-1}A(z))$: variable Bandpass
$\frac{-\propto +z^{-1}}{1-\propto z^{-1}}$; $\lvert\propto\rvert < 1$	$\sum_{0\le i\le N} h_i z^{-i}$	**0**	**1**	$G(z) = H(-A(z))$: variable Highpass
$\frac{-\propto +z^{-1}}{1-\propto z^{-1}}$; $\lvert\propto\rvert < 1$	$\sum_{0\le i\le N} h_i z^{-i}$	**1**	**1**	$G(z) = H(z^{-1}A(z))$: variable Bandstop

The parameter ∝ is called the first order warping coefficient and its value determines the cut-off frequency of the APT-VDF filter. Consider an N^{th} order lowpass prototype filter with cut-off frequency f_{co}, if $0 <\propto< 1$,then the resultant cut-off frequencies are lower than f_{co}. For $\propto= 0$, the transfer function of the APT-VDF filter is equal to the original transfer function of the prototype filter. If$-1 <\propto< 0$ then the resultant cut-off frequencies of the APT-CDF filter are higher than f_{co}. The parameter ∝ can be expressed as

$$\propto= \frac{sin\left[\left(f_{co} - f_c\right) * \pi/2\right]}{sin\left[\left(f_{co} + f_c\right) * \pi/2\right]}$$

where f_c is the cut-off frequency of the desired APT-VDF filter.Given a desired frequency response specifications, Matlab filter design tool can be used to obtain the prototype filter coefficients.

2.5.2 Floating-point to Fixed-point conversion

The APT-VDF architecture has been implemented in a Xilinx Virtex5 XC5VLX50T FPGA (speed grade 1) using fixed-point representation. Herein, we consider the generalized fixed-point number representation [WL,FL], where WL and FL correspond to the word length and the fractional length of the number, respectively. The difference IL=WL-FL is referred to as the integer length of the number. The word length and the fractional length of the input operands were set to 16 bits and 14 bits, respectively. To perform the fixed-point conversion, all arithmetic operations and floating-point variables of the APT-VDF filter are converted into fixed-point representation. Using the NumericTypeScope window, we are able to view the dynamic range of the filter's input/output data in the form of a log2 histogram, as depicted in Figure 26. The minimum integer word length is calculated under large amounts of simulation data. After that, the fractional word length is chosen through extensive simulation and tolerable error limit. In this work, the root mean square error (RMSE) of output data between floating-point filter and fixed-point filter is evaluated and it is considered as an optimization criteria (see Figure 35).

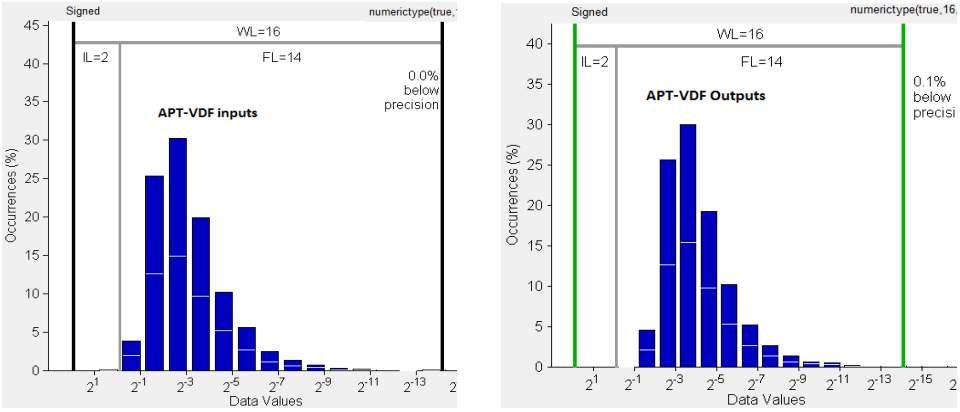


Figure 35 APT-VDF input/output data samples profiling

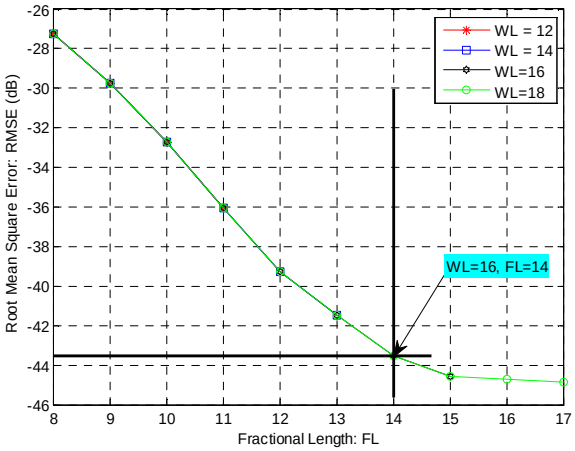


Figure 36 RMSE analysis versus word length and fractional length

The effects of different precisions on the APT-VDF filter magnitude responses are given in Figure 37 and Figure 38.

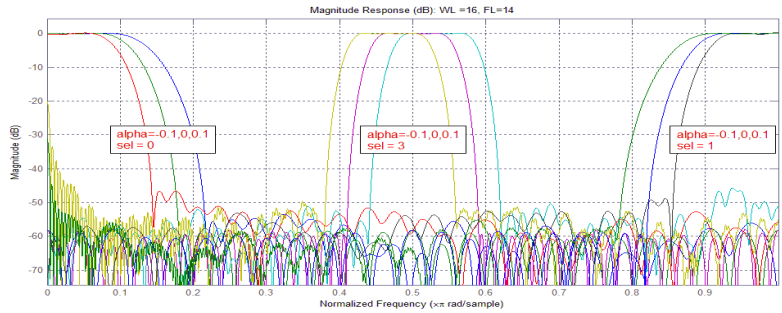


Figure 37 APT-VDF filter magnitude responses (WL=16, FL=14) versus alpha and sel

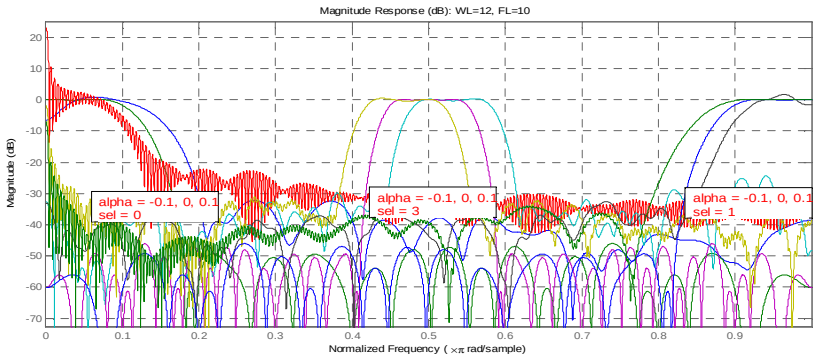


Figure 38 APT-VDF filter magnitude responses (WL=12, FL=10) versus alpha and sel

2.5.3 VHDL Implementation of the APT-VDF filter

The APT-VDF filter has to be implemented in such a way that the design has a static (Fixed, re-used) region and a reconfigurable region which depends on the *sel* parameter in the latter case. In this work, we assume that the parameter ∝ is known and fixed. The static part of the APT-VDF filter contains the prototype filter structure and the all-pass filter given the fact that the parameter ∝ is known. Both filters coefficients are given as constants in the implementation instead of giving them as inputs. The reconfigurable region of the APT-VDF filter contains just the minimum logic that is necessary to each *sel* parameter value. The VHDL code of the APR-VDF filter is written in such a way that it is reusable. By changing the order *N*, word length WL, and fractional length WL, an APT-VDF filter of any order and word length can be implemented. ModelSim tool is used to simulate the designed APT-VDF filter. Input stimulus is generated using Matlab, and the samples are written into a test file. The latter file is used as input of the testbench. Simulation results are shown in Figure 39.

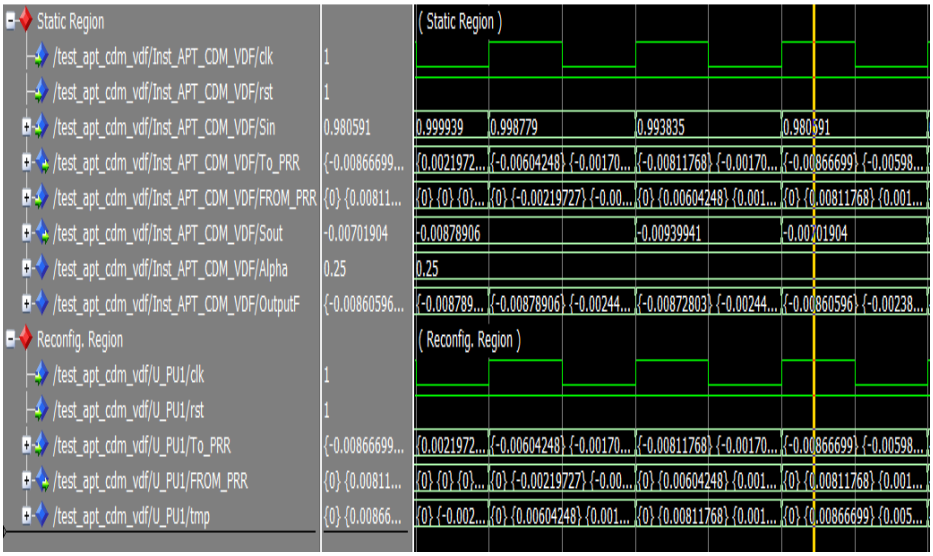


Figure 39 Output of Static and Reconfigurable Regions of APT-VDF filter in ModelSim.

2.5.4 Hardware Architecture Description

The hardware architecture of the proposed dynamic partial reconfiguration of APT-VDF filter is shown in 0. This architecture was built on ML550 development board and designed using ISE 14.7, XPS 14.7, and PlanAhead 14.7 environments. The proposed architecture contains the following components: Microblaze processor, processor local bus (PLB), memory BRAM, local memory bus (LMB), universal asynchronous receiver transmitter (UART RS232), multi-channel external memory controller (MCH EMC), and five general purpose input/output (GPIOs), true dual-port Ram, internal configuration access port controller, and our APT-VDF filter. The latter communicates with Microblaze via GPIO. The UART is integrated to allow the communication between the Microblaze and the RS232 interface of the board. All the peripherals communicate with the Microblaze via the PLB bus. The memory space of the BRAM is configured to be 16 KBytes. The on-chip dual-port RAM is configured to 128 Kbytes and it is used to store the partial bitstream files. The host PC is responsible for transferring those bitstream files to the Microblaze through the UART. The ICAP-DMA (Internal Configuration Access Port - Direct Memory Access) controller is a block that we have developed in our lab in order to take advantage of the 32bit modeofvirtex5. The goal is to get closer to the theoretical throughput of the ICAP capacity, 400MByte/s (ICAP running at a maximum frequency of 100MHz). The Microblaze is only used for the setup phase, after that, the ICAP-DMA controller works autonomously and acts like a DMA for partial bit stream files transfer between the dual-port RAM and the ICAP component. The ICAP-DMA controller is connected to the MicroBlaze through the GPIO. The ICAP component is configured in 32bits mode. Specific registers store the start addresses and the offset of the physical memory where partial bitstream files are stored in dual-port RAM.The main program, which is executed by the processor, is developed using the device drivers of each peripheral. The following figure explains the program execution procedure when the Microblaze processor starts up.

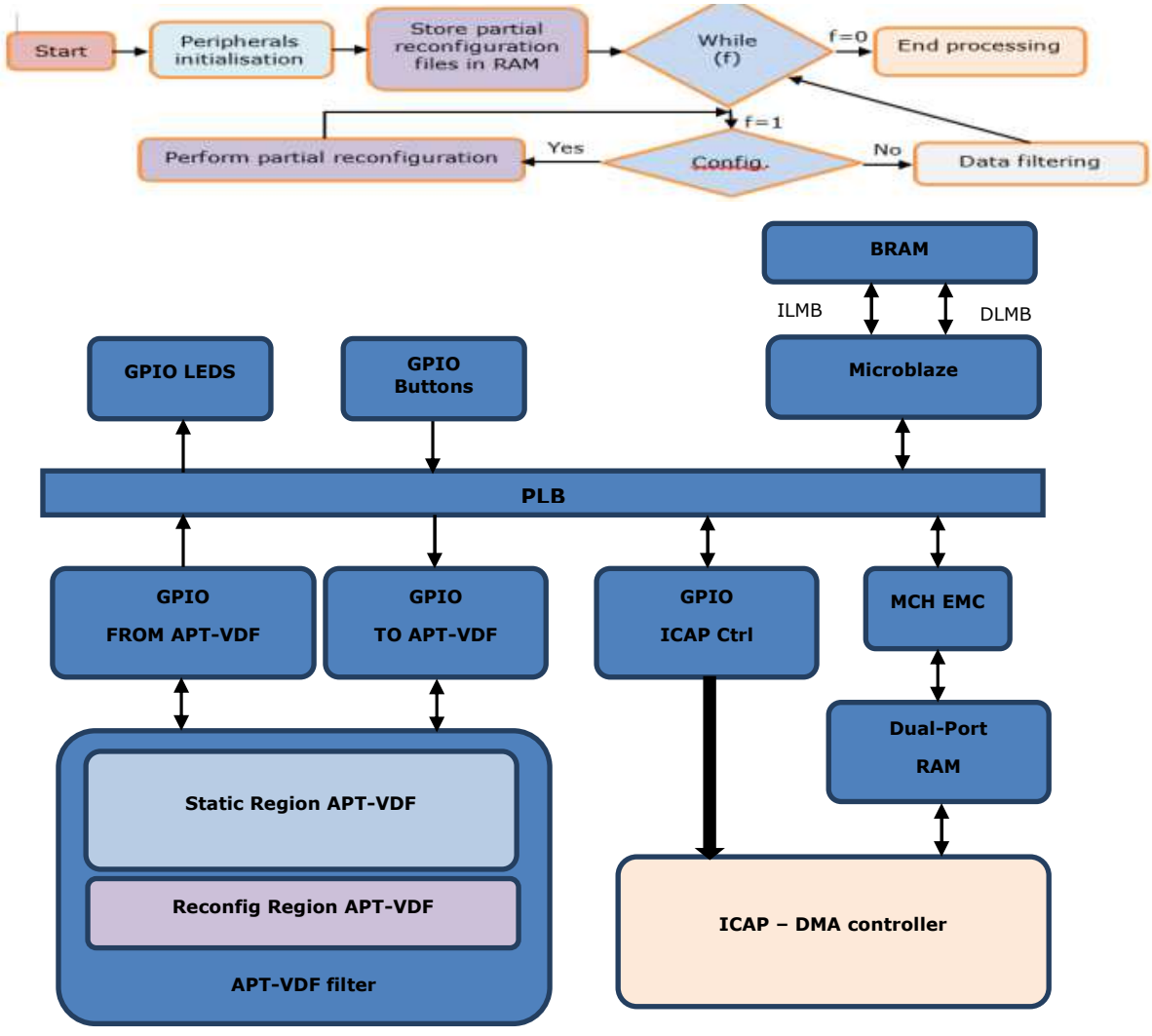


Figure 40 Hardware architecture of the embedded system

2.5.5 Experimental Setup

We have performed experiments on the Virtex-5 FPGA to implement APT-VDF filter and to study the FPGA energy consumption behaviors. The ML550 development board from Xilinx is well suited to power consumption measurement for several reasons. The FPGA on this board is a XC5VLX50T which is a Virtex5 LX series. This board provides us with 5 power rails (core, IOs, peripherals) and current sense resistors which would simplify the experimental measurement. The recommended Virtex5 core voltage, designated V_{CCINT}, is 1.0 ± 10%V. Depending on the I/O standard being implemented, the Virtex5 I/O voltage supply, designated V_{CCO}, can vary from 1.2V to 3.3V. Moreover, Xilinx defines an auxiliary voltage, V_{CCAUX}, which is recommended to operate at 2.5±10%V to supply FPGA clock resources. The board hosts a two header connector which provides test points for the ML550 power regulators. Moreover, to measure different currents drained by the FPGA, the ML550 board contains a series shunt 10mΩ± 1% 3W Kelvin current sense resistors on each voltage regulator lines. Thus, the current will be the voltage across the shunt resistor divided by the resistance value itself. Since the sensitivity of the V_{CCINT},V_{CCO}, and V_{CCAUX} sensors are pretty low (0.5−2mV), voltage amplifiers are needed. To this end, we have used integrated instrumentation amplifiers AD620, from Analog Devices. The AD620 has a feature to increase gain between 1 − 10.000 times with an external resistor. Those amplifiers allow regulating the gain only by changing a single resistance, called RG. We wanted to reach a voltage of about 100−400mV,at the output of the voltage amplifier then, according to the components availability of the laboratory, was established gains of about 100 and1000respectively for the V_{CCINT} and V_{CCO} using resistances of 483 Ω, and 49 Ω. Figure 41shows the connections between ML550 sensors and amplifiers. The output voltage pins from the board are the differential output from the sensors.

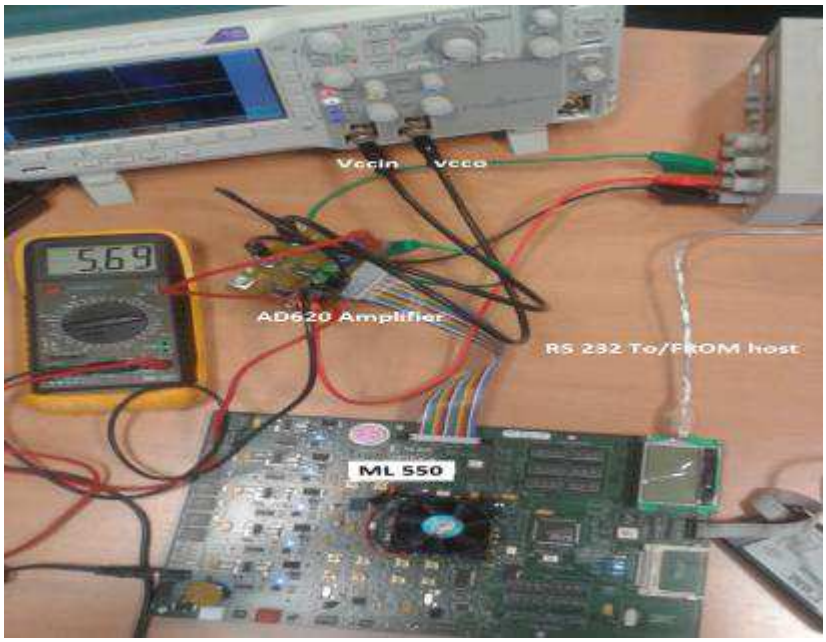


Figure 41 ML550 development Board with AD620 amplifier

2.5.6 Validation results

In this section, the implementation results and power consumption measurements of the APT-VDF filter are given with the help of a suitable design example. Herein, all mentioned frequencies are normalized with respect to half of the sampling frequency. Consider a prototype lowpass filter where the cut-off frequency, the transition bandwidth, the passband, and the stopband ripple specifications are 0.08, 0.14, 0.8 dB, and -40 dB, respectively. Using the filter design and analysis tool and direct-form FIR structure, the order of generated prototype filter is equal to *N=21*.

Table 19presents the experimental FPGA reconfiguration time needed to perform APT-VDF filter reconfiguration. Three reconfiguration approaches are used:

- Full FPGA reconfiguration: we use JTAG connector to configure the FPGA with a total pre-made bitstream.

- External partial FPGA reconfiguration: we use JTAG connector to configure just the reconfigurable region of the APT-VDF filter with a pre-made partial bitstream
- Internal partial FPGA reconfiguration: we use internal configuration access port (ICAP-32bits) to configure just the reconfigurable region of the APT-VDF filter with a pre-made partial bitstream.

Table 19 Bit stream file size and reconfiguration time on Virtex 5 xc5vlx50T

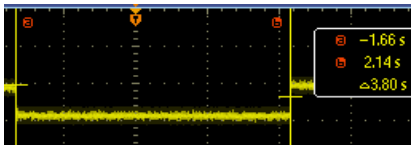
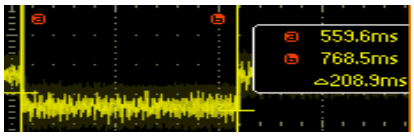
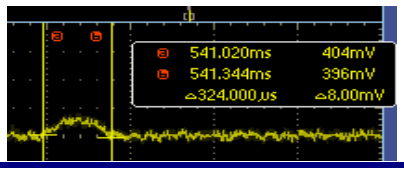
Reconfigurable IP	Bitstream size	Reconfig. time	Oscilloscope outputs
FPGA Full-reconfiguration (JTAG)	1716 KBytes	3.80 s	
APT-VDF Partial-reconfiguration (JTAG)	94.464KBytes	208.9 ms	
APT-VDF Partial-reconfiguration (ICAP)	94.464KBytes	324 µs	

Table 20 summarizes the key (post-place-and-route) implementation results of the reconfigurable region when the parameter *sel* is equal to "01" and "11", respectively. The results are coherent with our expectation given the fact that when *sel* is "01" the generated APT-VDF filter is equivalent to highpass filter. However, when *sel* is "11", the generated APT-VDF filter is equivalent to a bandpass filter, which requires to insert (21 * WL) delay units.

Table 20 FPGA physical resources of the reconfigurable region

FPGA resources	APT-VDF filter ($\propto = 0.25$, sel="01") (Reconfigurable Region)	APT-VDF filter ($\propto = 0.25$, sel="11") (Reconfigurable Region)
LUT / FD_LD	315 / 0	336 / 336
SliceL/SliceM	67/23	77/26
Nb of Frames	16	16
Nb of Frame Region	2	2
Bitstream size	94464 Bytes	94464 Bytes

The overall resource required to implement the embedded system is shown in Table 21. Moreover, the static and dynamic power consumption of the design mapped on FPGA can be estimated using the Xilinx XPower analyser tool. Figure 42 and Figure 43 report the power consumption of the FPGA core during total reconfiguration step. The power consumption is given by V_{CCINT} value. During total reconfiguration, the power consumption of the FPGA core is stable around 210 mW, otherwise it is around 370 mW. During partial reconfiguration phase, the power consumption of the FPGA core is equal to 440 mW.

Table 21 Total FPGA physical resource usage of the embedded system

FPGA resources	APT-VDF filter ($\propto = 0.25$, sel="01")	APT-VDF filter ($\propto = 0.25$, sel="11")
BUFGs	2	2
DSP48Es	14	14
ICAPs	1	1
External IOBs	13	13
RAMB36_EXPs	33	33
Slices	2364/7200	2427/7200
Slice Registers	3843/28800	4179/28800
Slice LUTS	4850/28800	4998/28800
Static power	450 mW	450 mW
Dynamic power	256 mW	270 mW
Total power	707 mW	720 mW

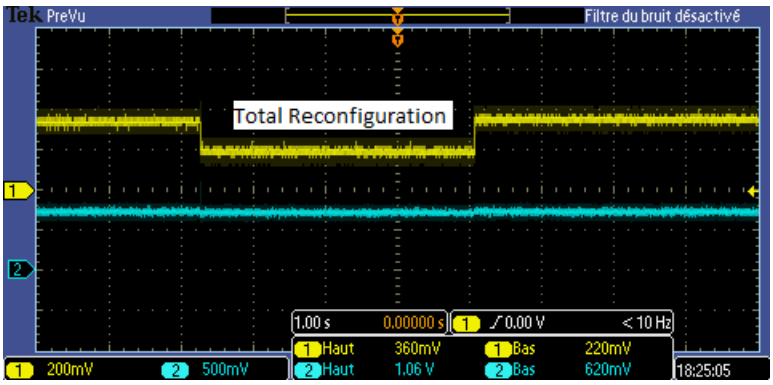


Figure 42 FPGA core power consumption during total reconfiguration

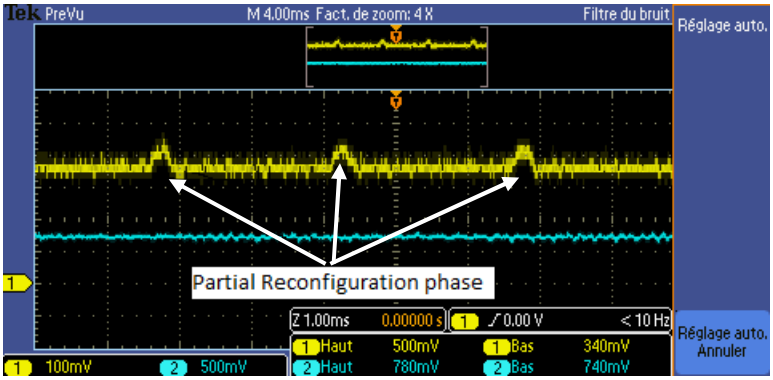


Figure 43 FPGA core power consumption during partial reconfiguration

2.5.7 Conclusions

We have presented an implementation of a variable digital filter (VDF) with unabridged control over cutoff frequency, using FPGA dynamic partial reconfiguration. In this proof-of-concept, three main conclusions can be drawn:

- FPGA dynamic partial reconfiguration is an efficient design technique which permits to change a part of the devices while the rest of an FPGA is still running. Moreover, this technique can reduce dynamic and static power consumption in comparison with the well-known parametrization design approach.
- The reconfiguration time is very small (around 324 µs for partial bitstream size equal to 95Kbytes).
- Very small power consumption overhead during partial reconfiguration phase.

3 CONCLUSIONS

The deliverable D7.4 has detailed the proof-of-concepts of the selected implementations describing the required interfaces. This document has also described the final results and analysis of the trials related to the following topics:

- Relaying and Device-to-Device communications
- Interference aware receiver of DL MU-MIMO CoMP
- Carrier aggregation
- Wi-Fi offloading
- FPGA reconfigurability for low-power APT-VDF filter implementation

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GLOSSARY

ACRONYM	DEFINITION
3GPP	Third Generation Partnership Project
AAA	Authentication, authorization and accounting
ACLR	Adjacent Channel Leakage Ratio
AP	Access point
API	Application programming interface
APT	All-pass transformation
BS	Base Station
CA	Carrier Aggregation
CC	Component Carrier
CCDF	Complementary Cumulative Distribution Function
CW	Continuous wave
D2D	Device to Device
DC	Direct Current
DL	Downlink
DMA	Direct memory accesss
DTC	Digitally Tunable Capacitor
eMBMS	Enhanced Multimedia Broadcast Multicast Service
eNB	evolved Node B
E-TM	E-UTRA test model
E-UTRA	Evolved Universal Terrestrial Radio Access
FDD	Frequency Division Duplex
FL	Fractional length
GPIO	General purpose input output
GUI	Graphical user interface
HetNET	Heterogeneous Network
HSS	Home subscriber server
ICAP	Internal configuration access point
IEEE	Institute of Electrical and Electronics Engineers
LMB	Local memory bus
LTE	Long Term Evolution
LTE-A	Long Term Evolution - Advanced
MADM	Multiple attribute decision making
MCHEMC	Multi-channel external memory controller

MCLA	Monopole coupled loop antenna
MME	Mobility management utility
MO	Mobile operator
OBO	Output back-off
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
PCB	Printed Circuit Board
PLB	Processor Local Bus
PLMN	Public Land Mobile Network
PoC	Proof of Concept
RF	Radio Frequency
RMSE	Root mean square error
RX	Reception
SC	Small Cell
SNR	Signal to Noise Ratio
TDD	Time Division Duplex
TVWS	Television White Space
TX	Transmission
UART	Universal asynchronous receiver transmitter
UE	User Equipment
UL	Uplink
VDF	Variable Digital Filter
WL	Word length
WP	Work Package